KNU 경북대학교
KYUNGPOOK NATIONAL UNIVERSITY

Fabrication Techniques for Quantum Devices

Part 1

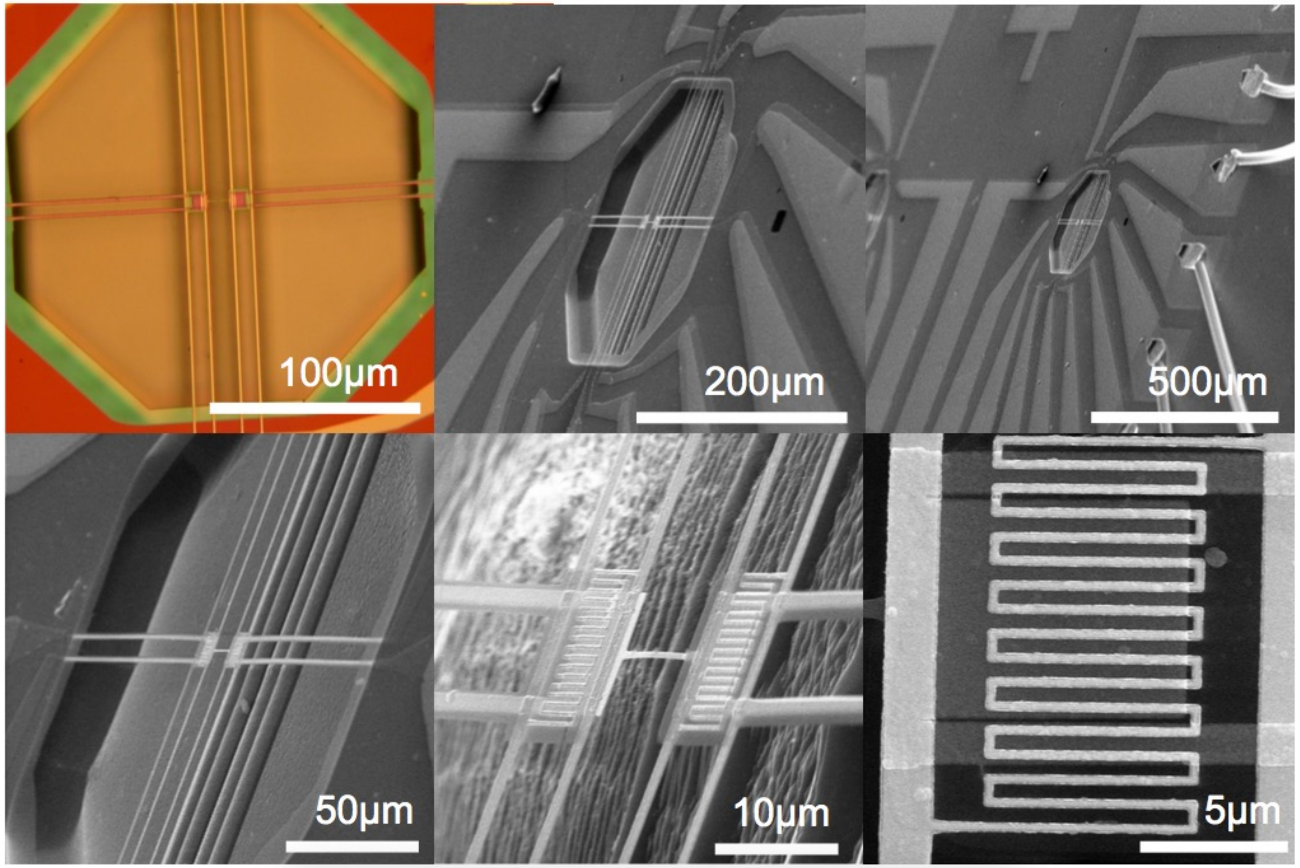
The 13th School of Mesoscopic Physics:
Mesoscopic Quantum Devices
23 MAY 2024

Dep. Physics Kyungpook Nat. Univ.

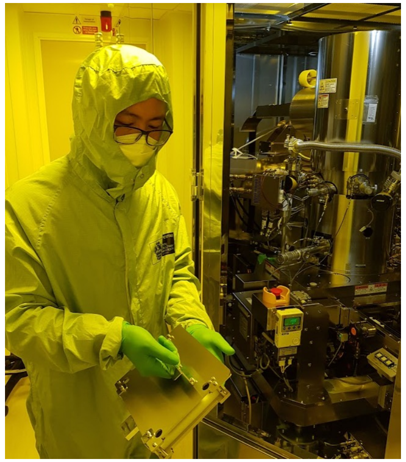
Myunglae Jo


The 19th Workshop on Nanoscale and Mesoscopic Systems
Nanowires and Nanotubes
May 22 – 23, 2009
KIAS(Korea Institute for Advanced Study)
경영
고등과학

My journey

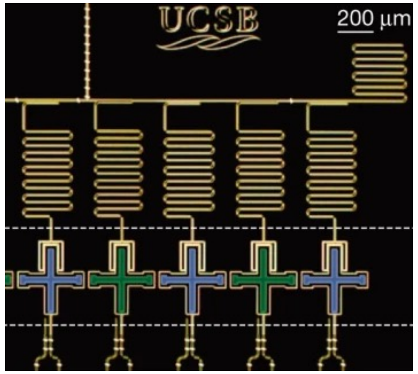


- NEMS thermal property
- So called Majumdar device
- Year 2008
- Drawing something small

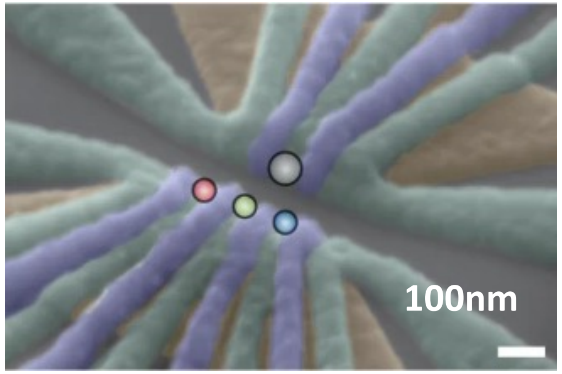


Quantum devices

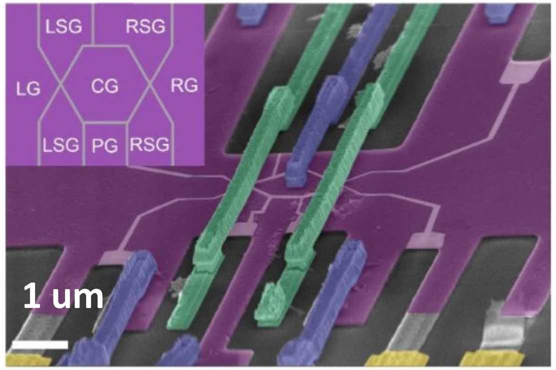
- “A device whose functionality or principle of operation depends essentially on quantum mechanical effects” [1]
- Qubit, quantum sensors, photonics, quantum dots etc



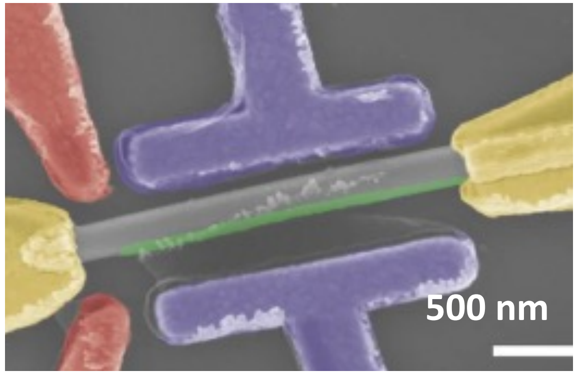
SC qubit [2]



Quantum dots [3]



Graphene interferometer [4]



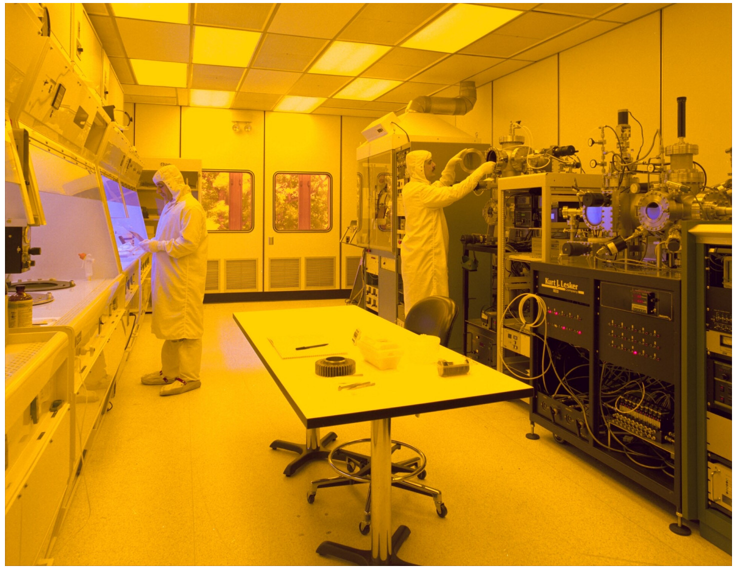
Majorana zero mode [5]

[1] Encyclopedia of Condensed Matter Physics, 2005
[2] Nature 519, 66–69 (2015)[
[3] Nature 608, 682–686 (2022)
[4] arXiv:2402.12432
[5] Nature 556, pages74–79 (2018)

Why smaller and cleaner?

- Length scale: mean free path, coherence length etc.
- Confining or manipulating quantum particles (electron, ion, spin…)
- Unwanted defects density
- Quantum phenomena at reduced scale
- As born nanomaterials

So inevitably CLEAN ROOM [1]



Wikipedia

Plan of this lecture

- Nomenclature and basic concepts
- Instead of listing techniques, let’s explore case by case
- All the examples and description are leaning toward **Lab scale RnD** not industrial.

Key techniques and consideration

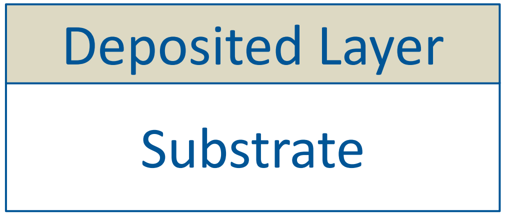
- Lithography
- Deposition
- Etching
- 2D assembly

- What is the smallest size?
- Required precision
- Additive? Or subtractive?
- Top down or bottom up?
- Functionality
- Compatibility

Typical micro/nano fabrication process

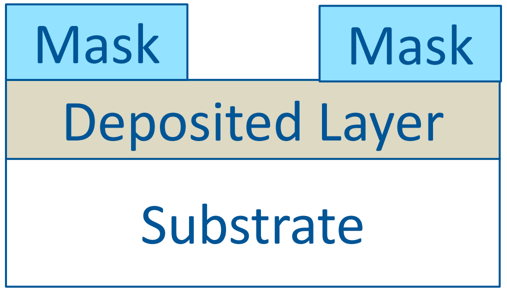
Substrate selection

- Material & Quality



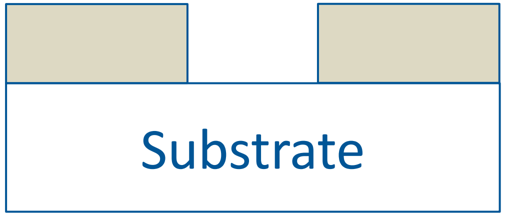
Additive process

- Chemical deposition
- Physical deposition



Lithography

- Expose & develop
- E-beam, Photo



Subtractive process

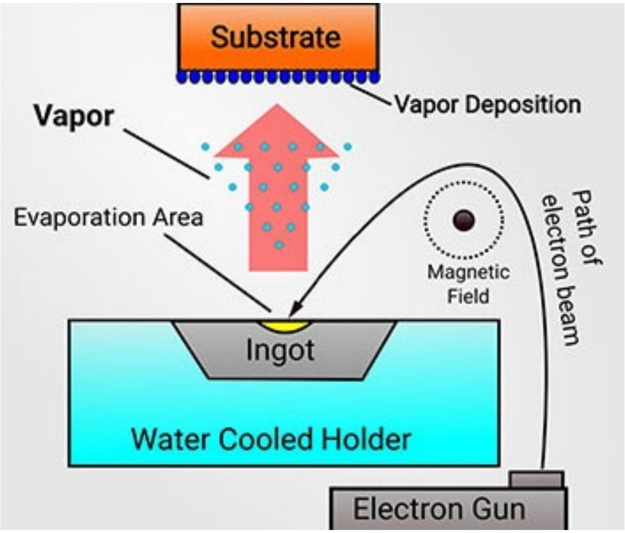
- Wet etch
- Dry etch

Additive process

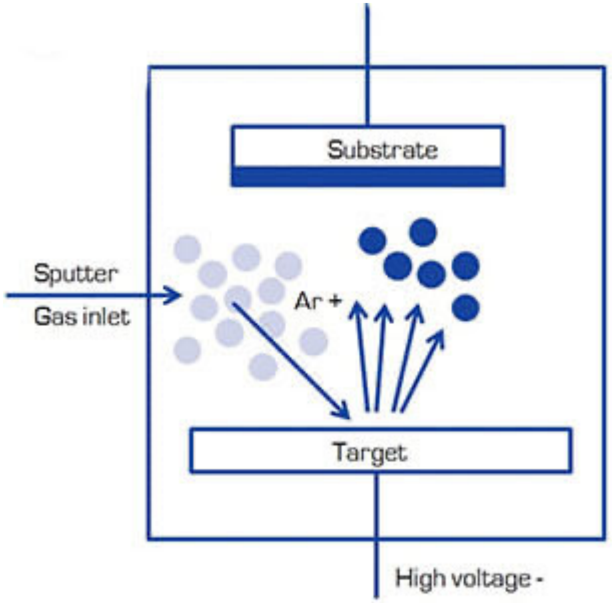
Image: https://www.performancecontracting.com/

- Industrial paint Coating
- Even
- Non-selective as it is

Physical Vapor Deposition



E-beam evaporation

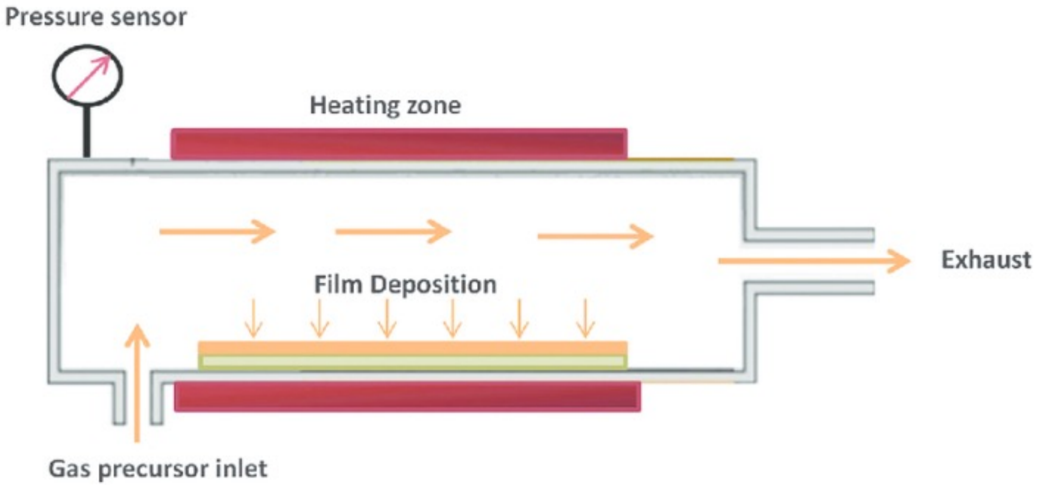


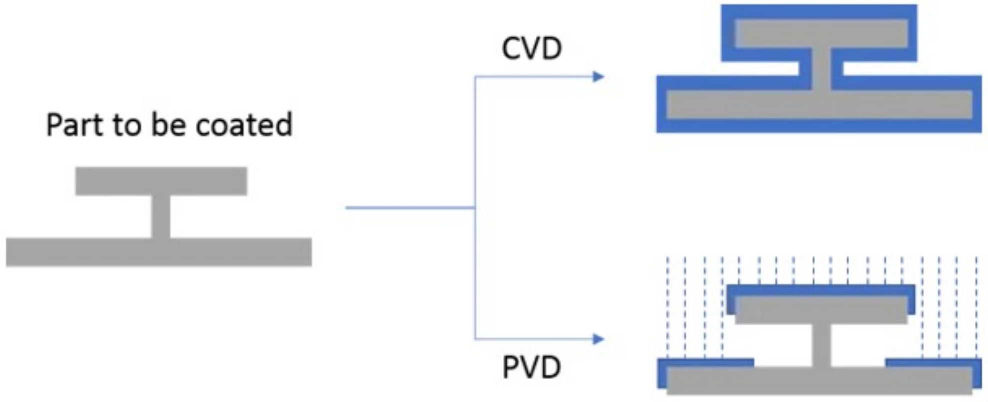
Sputter

- Directionality: shadow effect
- Directionality (better lift off) : evaporation > sputter
- Material purity: sputter > evaporation

Image: https://jingsourcing.com/p/b04-types-of-physical-vapor-deposition/

Conformal coating





- Chemical Vapor Deposition (CVD)
- Atomic Layer Deposition

- Chemical reaction, precursor
- Highly conformal coating (ALD> CVD)
- ALD: Layer by layer control
- Epitaxial growth possible

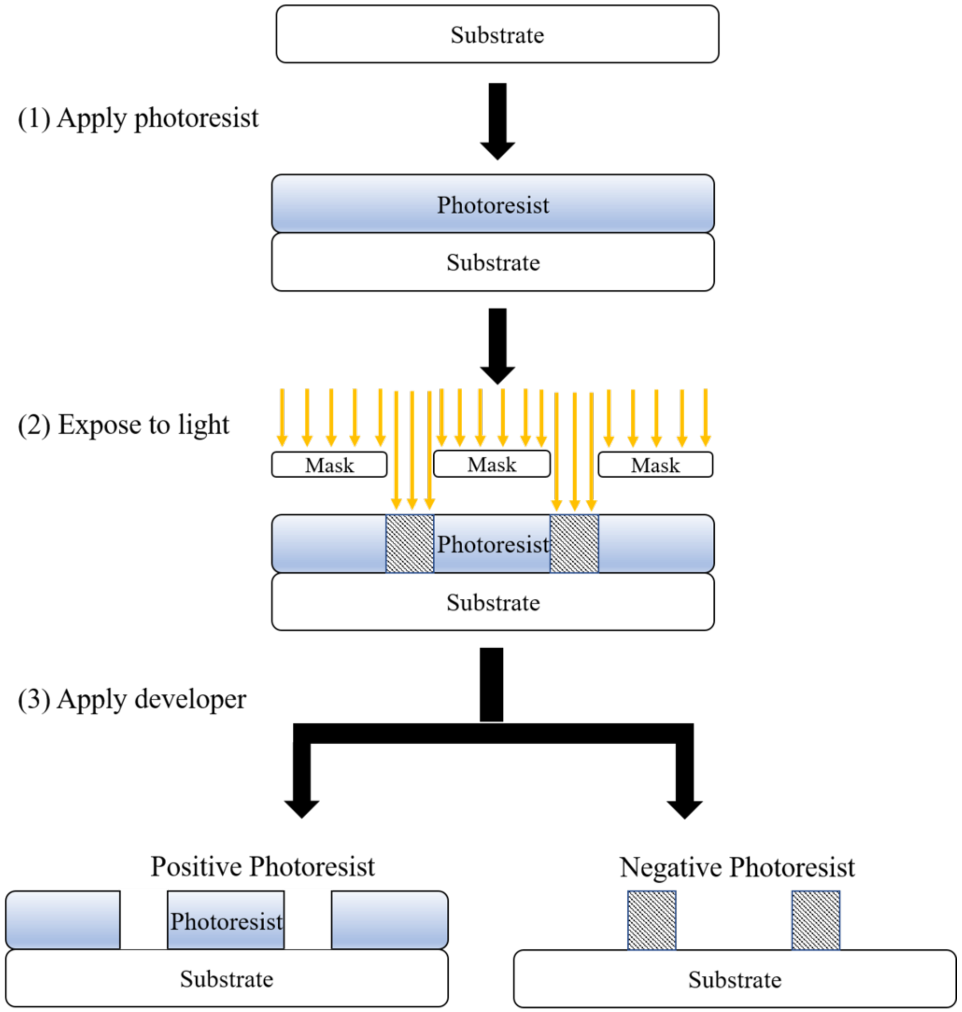
Image: J. Mater. Chem. C, 4, 4092-4124 (2016)
www.silcotek.com

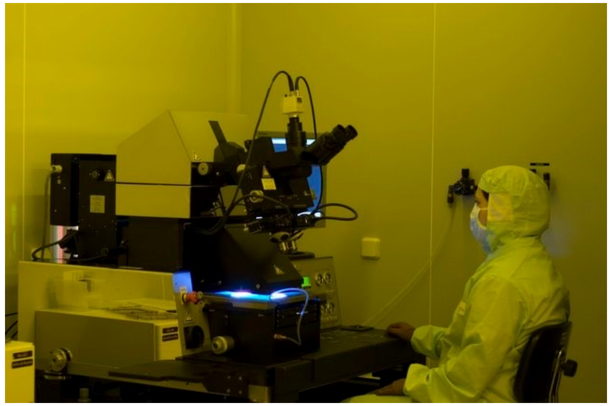
Lithography

- lithos: stone graphō: to write

Image: https://thekidshouldseethis.com/

Photo Lithography

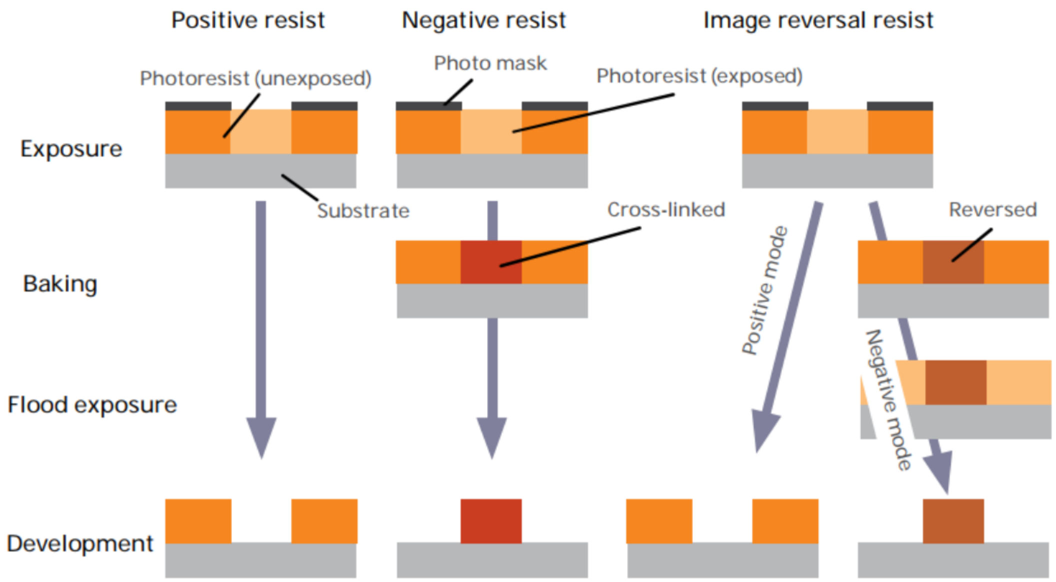


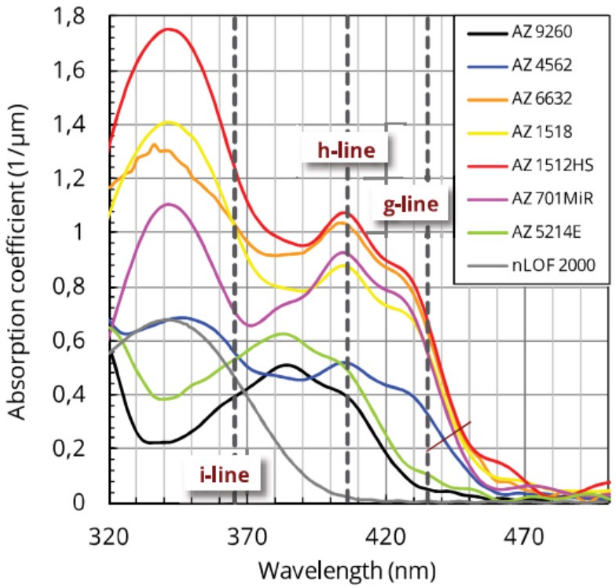


- Seeing (visible light), writing (UV) separated
- Direct observe and align
- Even coating is crucial: spin coating
- Lab level mask aligner (contact type)
- Up to 1um but 2um is more practical
- Alignment resolution 0.5 um

Image: Wikipedia
https://www.cenimat.fct.unl.pt/

Photo Resist





- Resin + photoactive substances + solvent
- Spin coating, spray coating
- Keeping 5-10 C storage preferred, but beware water condensation
- Yellow light: Do blue object looks blue instead of grey or black? Warning
- Ambient exposure test

Image: microchem

Developer

- Usually Aqueous-alkaline
- Metal Ion Free (MIF) organic TMAH: impurity, high-temperature process?
- Keep the container closed: Neutralization by CO_2
- MIC and MIF developer are not compatible
- Development is chemical reaction: temperature, concentration, agitation
- Thick resist (~10 um or higher): penetration depth of light should be considered

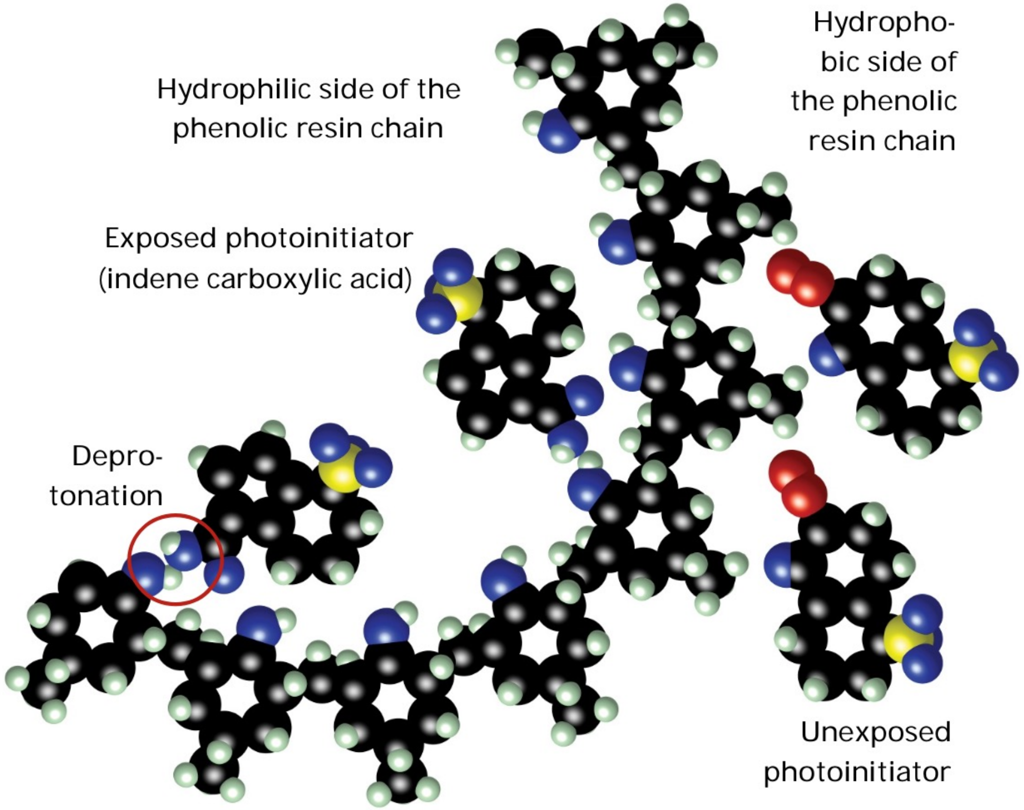
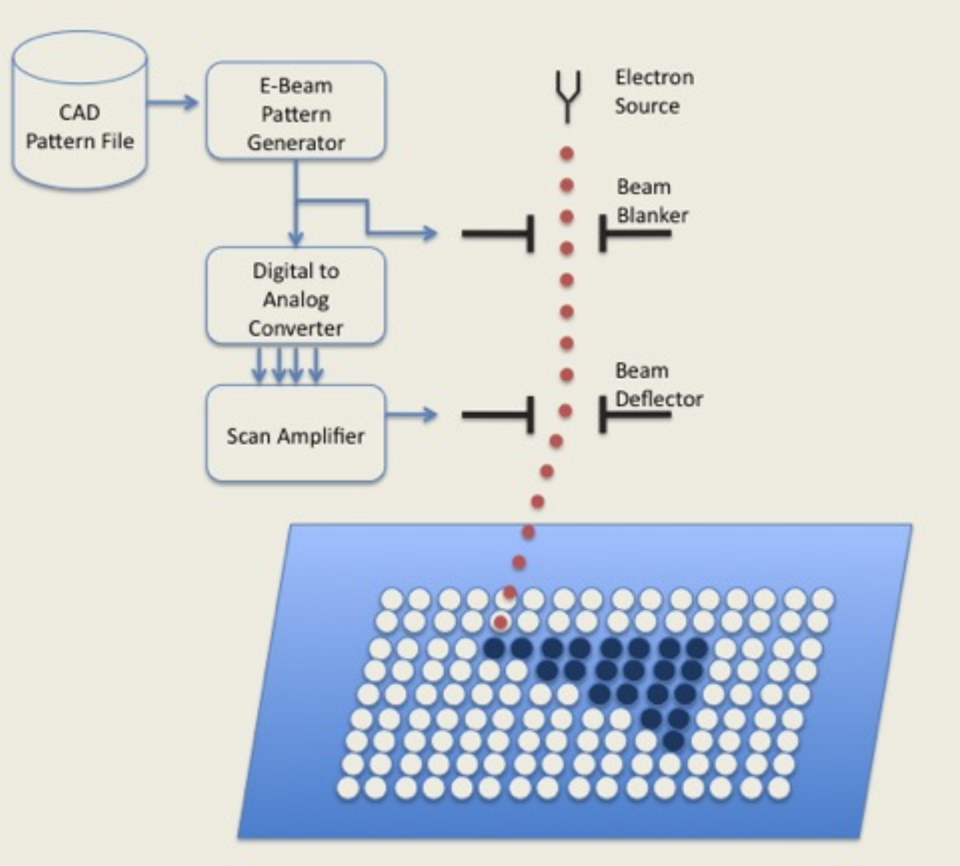
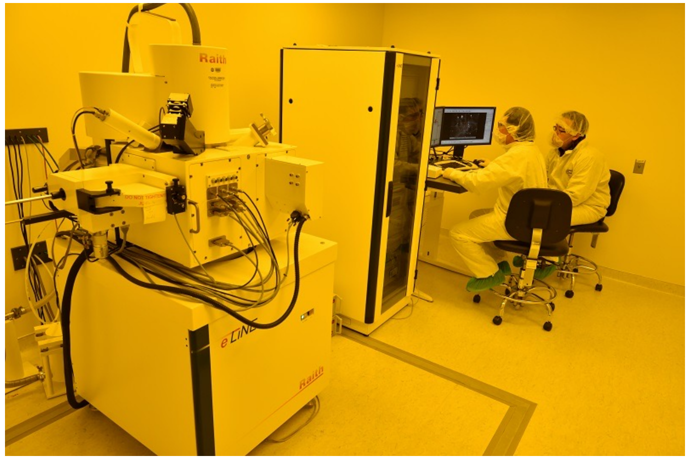


Image: microchem

E-beam Lithography



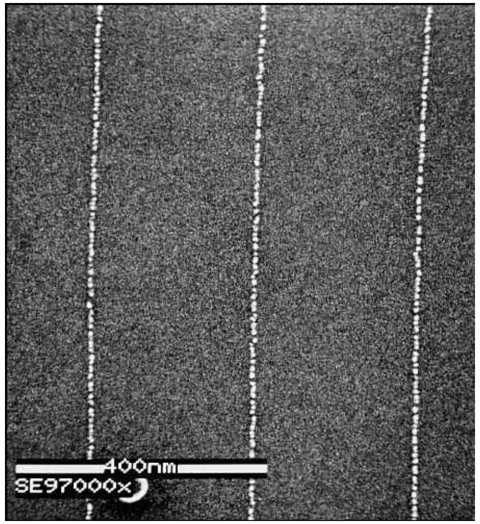


- Shorter wavelength, writing 10 nm
- point drawing, slow
- Electro magnetic optics: focus matter
- Seeing = writing = electron
- Maskless: non-flat substrate possible
- No Direct observe and align: align marker

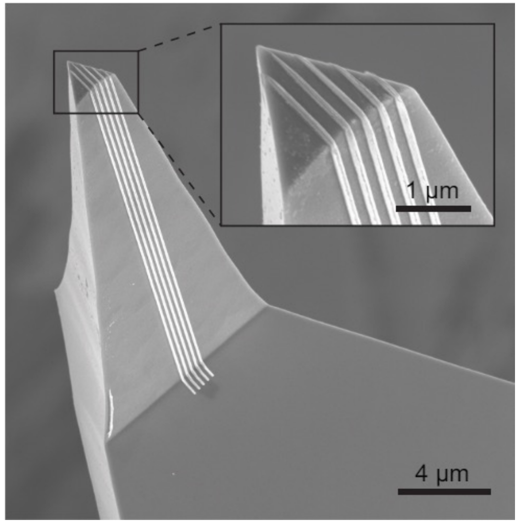
Image: https://ebeam.wnf.uw.edu/
https://www.nano.pitt.edu/node/482

E-beam Resist

- PMMA: positive, Excellent adhesion to most substrates, widely used
- ZEP: high resolution resist
- CSAR62 (poor man's ZEP)
- ma-N series: negative resist, DUV, good etch resistance



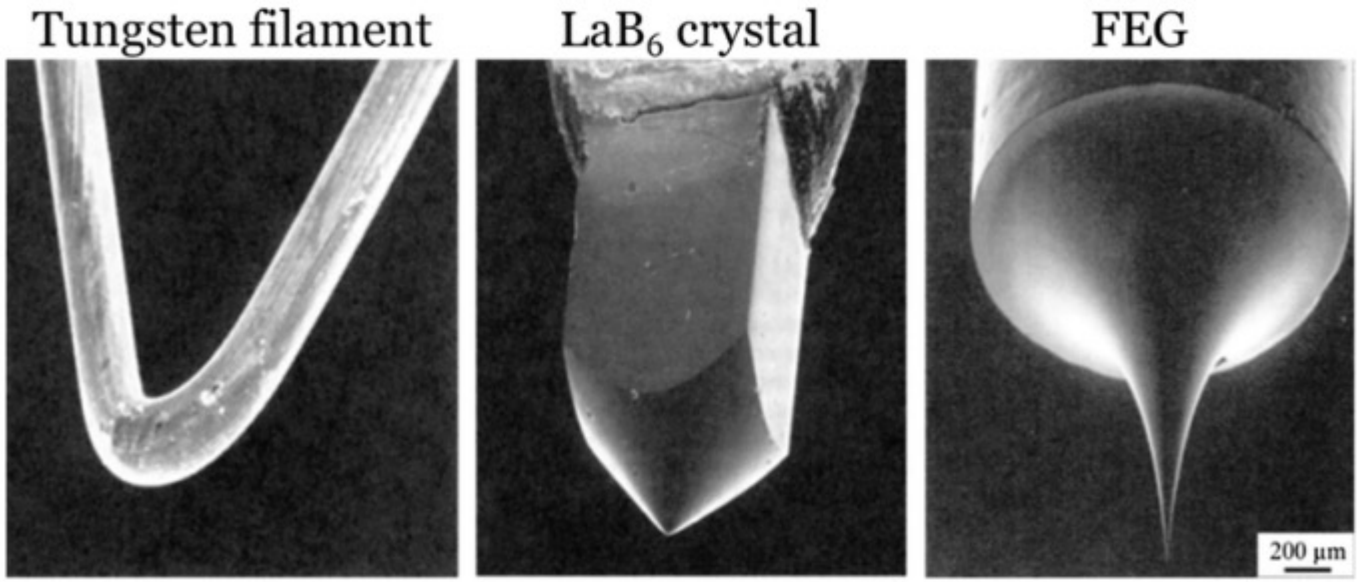
5nm Au line NPGS



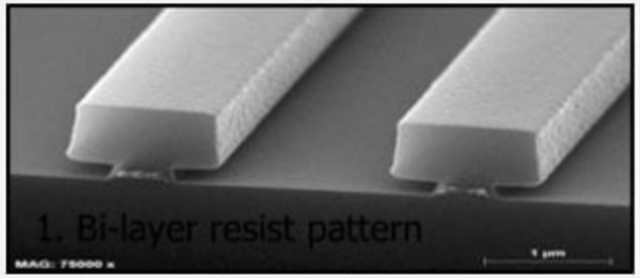
AIP Advances 13, 035208 (2023)

E-beam emission

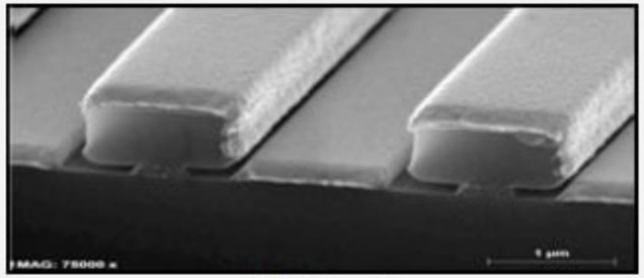
- Better resolution (as imaging): Field Emission > LaB_6 > Tungsten Thermionic emission
- Morphology + working principle
- Thermal FE has more stable current emission compared to Cold FE- > hence EBL



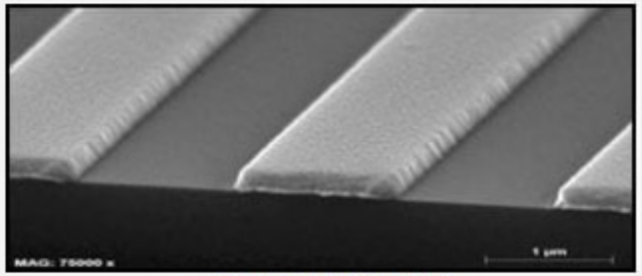
Lift Off Resist and Bilayer



1. Bi-layer resist pattern

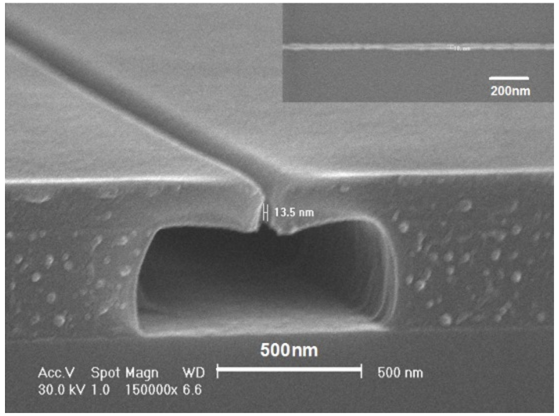


2. Metal Deposition



3. Clean solvent lift-off

- Thick film lift off, rotation and tilt
- Consider intermixing
- PMGI, LOR resist: developed in TMAH or KOH
- PMMA/MA copolymer with other positive e-beam resist
- Different molecular weight



PMMA/LOR

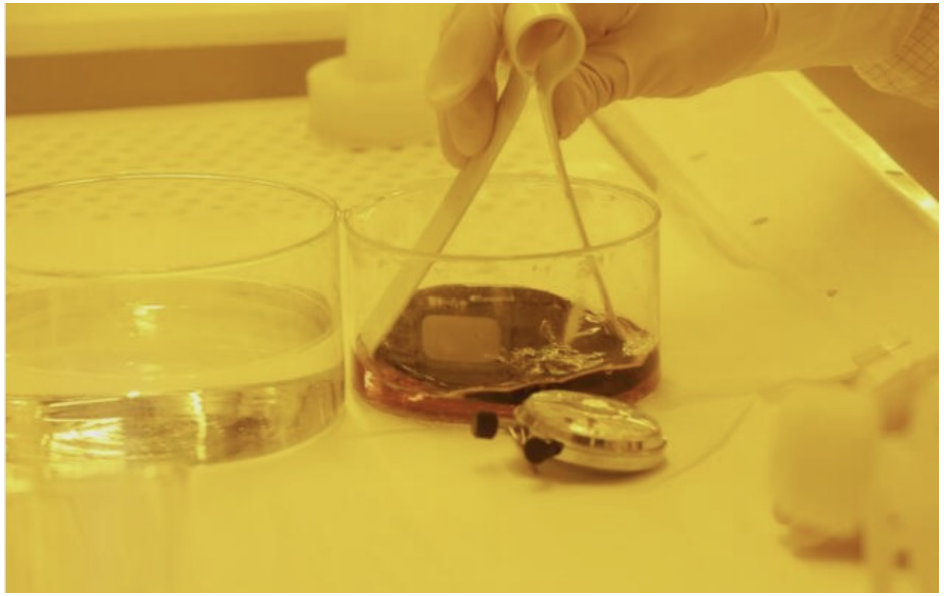
Image: Kayaku

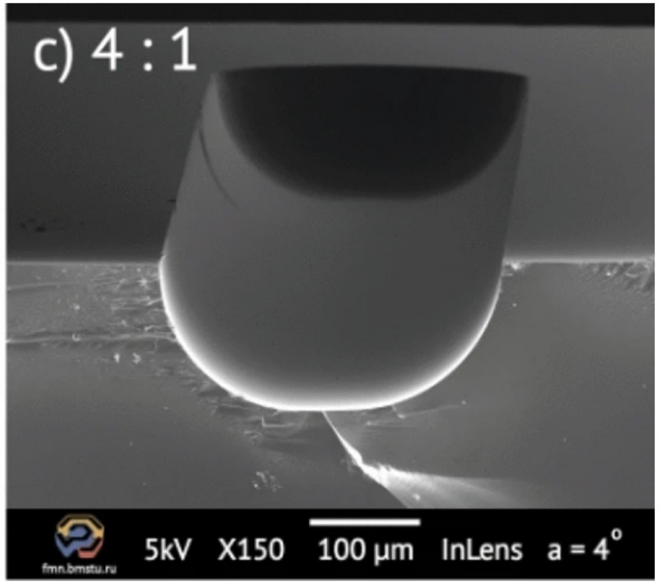
Subtractive (etch) Process

- Sand blaster with masking
- Even & Non-location-selective

Image: Youtube, Traditional Sandblasting PERFECT Headstones from Headstone Guy

Wet etch





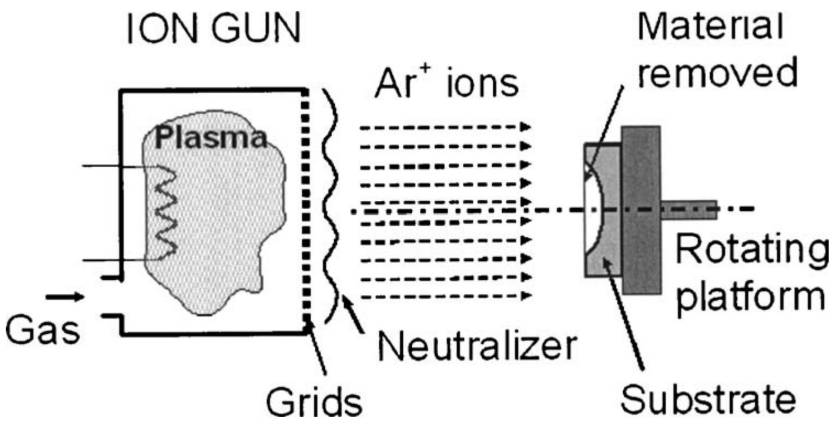
BOE etched Silica [1]

- All chemical etch (isotropic)
- High selectivity
- Not suitable for sub micrn

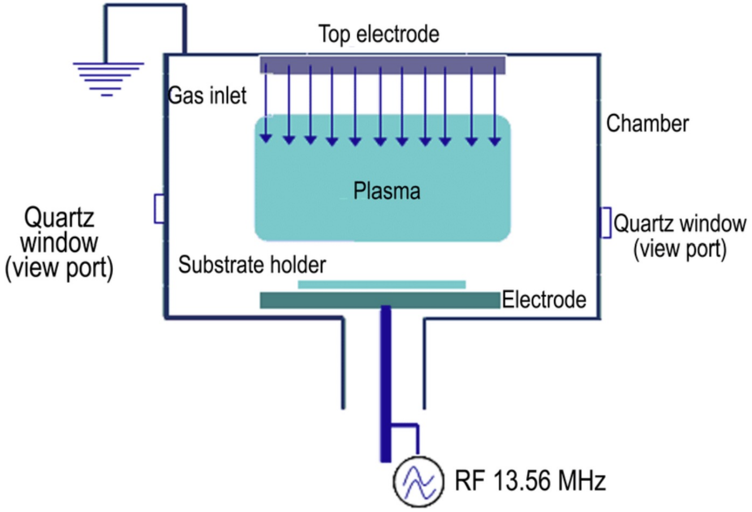
- High etch rate
- Some anisotropic (KOH)

Image: https://uwaterloo.ca/ , http://www.nff.ust.hk/
Sci Rep **13**, 5228 (2023)

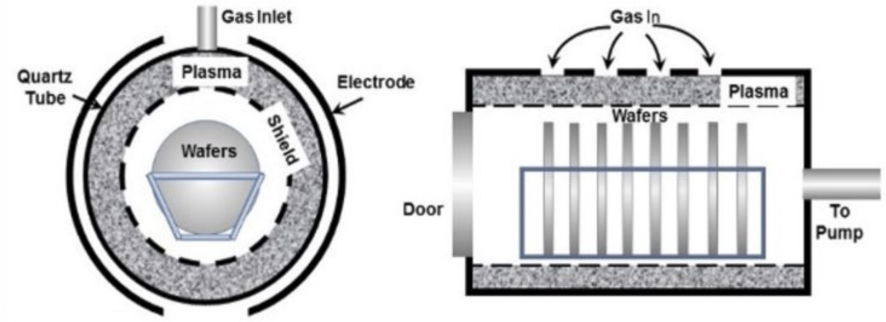
Dry etch



Ar milling



Reactive Ion Etcher (RIE)

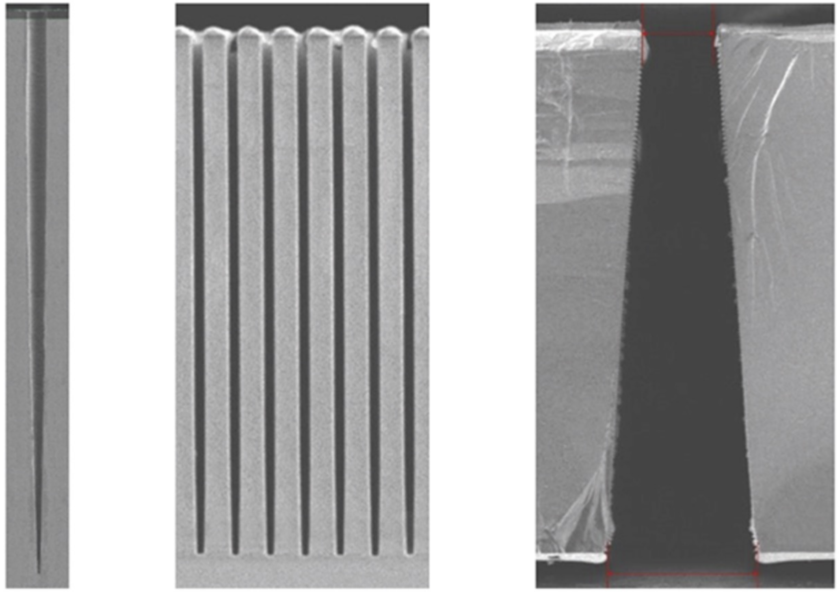


Barrel etcher, asher

- Pure mechanical to pure chemical
- Gas phase, directionality possible
- Lower selectivity
- Good resolution <100 nm

Image: Journal of Applied Physics 99, 094912 (2006)
MKS, Oxfords

Dry etch

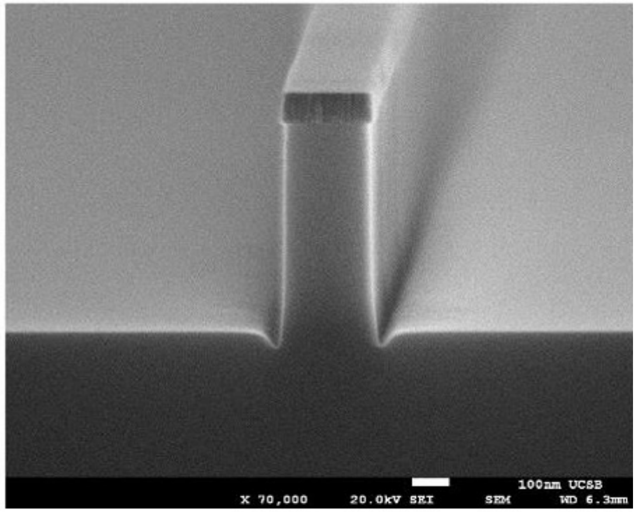


Positive taper
Depth: 400 µm

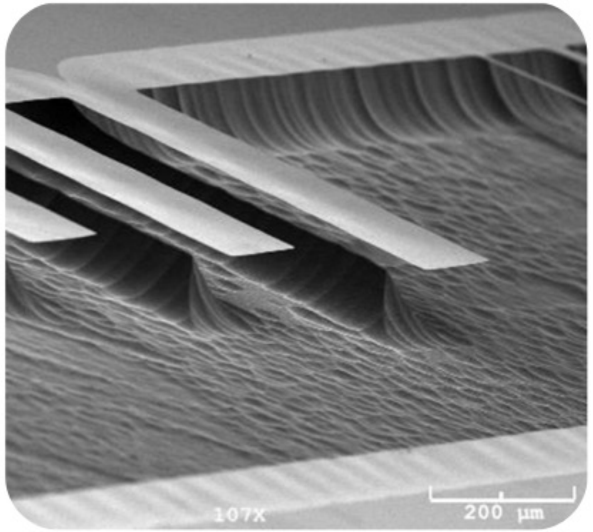
Vertical
Aspect ratio: >50

Reverse taper
Depth: 600 µm

Bosch process



RIE etched Silica



XeF2 etch

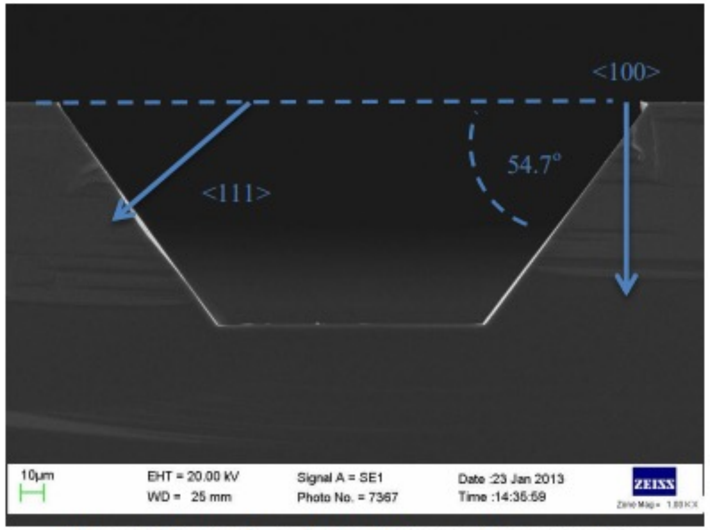
- Need to match gas to target material
- No drying related issue

- Precise etch rate control
- Some isotropic (XeF2, VHF)

Image: https://www.samcointl.com/ , UC Santa Barbara, Nanofab , https://www.kla.com/documents/XeF2-Intro-USLetter-Feb2023-KLA.pdf

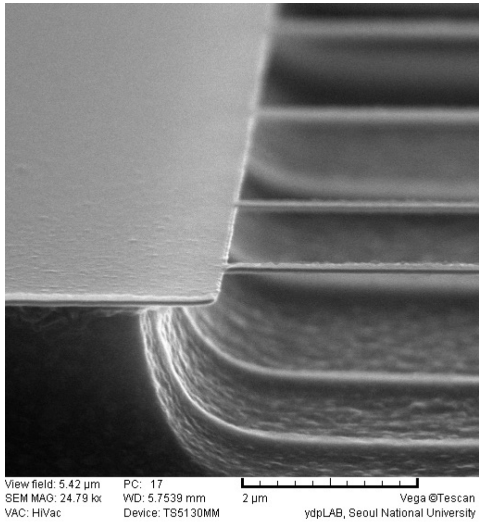
Directionality or anisotropy

- Chemical dominated = wet etch, plasma etch, XeF2 etch -> isotropic
- Physical dominated (or combined) = ion mill, RIE -> anisotropic
- Some rare cases: KOH Si etch, wet anisotropic, due to crystalline nature



250um wide trench, etched to 89.3um, <100> orientation

KOH etched Si [1]



Poor anisotropic RIE [2]

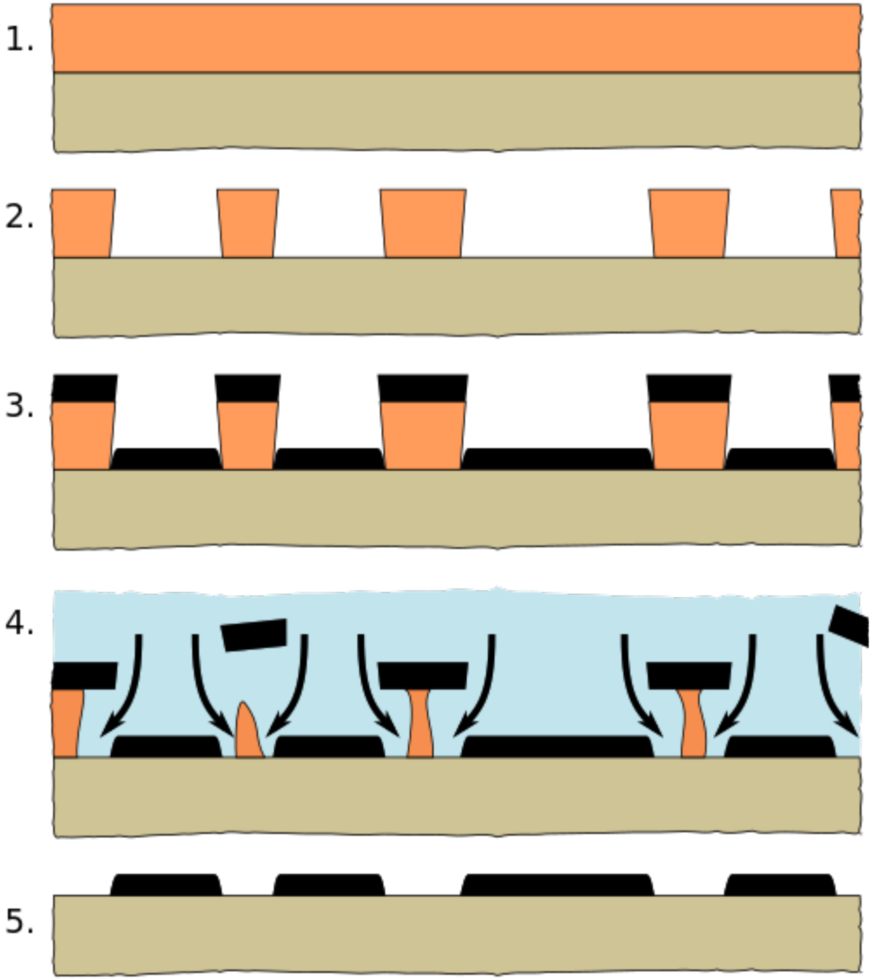
[1] www.nanofab.ualberta.ca
[2] from lecturer

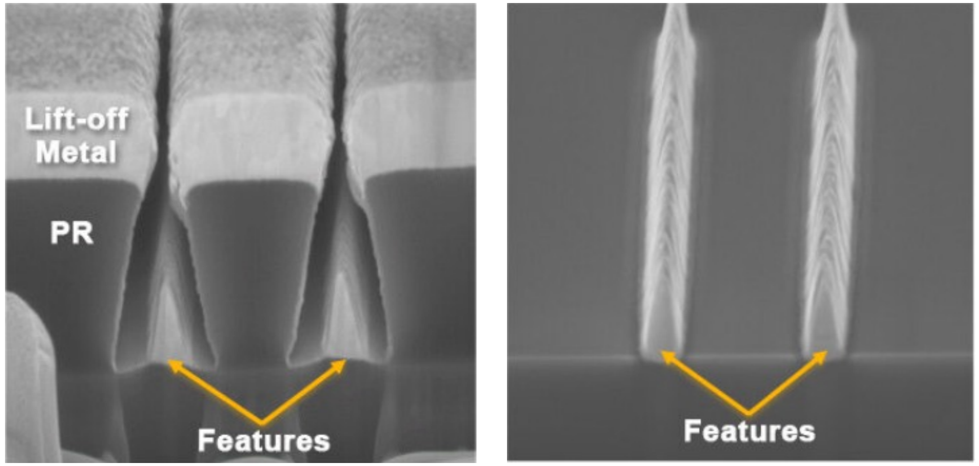
Lift off

- Painting with masking tape

[1] Youtube, How Racing Stripes Are Painted On A Car, from Business insider

Lift off

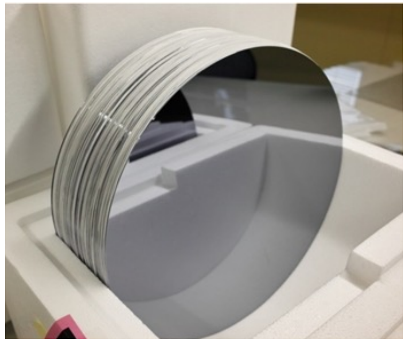




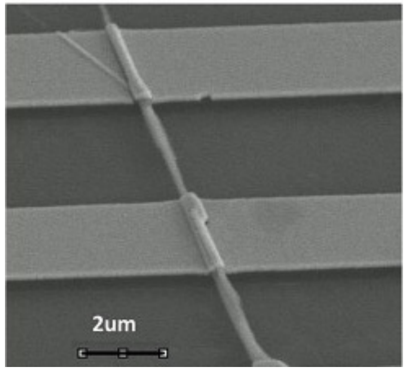
- Resist = mask or sacrificial layer
- Added layer can be patterned
- Double layer, undercut, LOR
- Sonic agitation, temperature

Image: https://commons.wikimedia.org/
https://classone.com/electroplating/metal-lift-off-process/

Nearly 2D



- Your substrate is flat: RMS <1nm for polished Si wafer

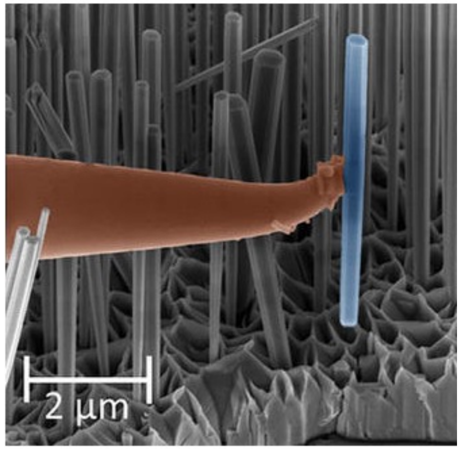


- Electrode metallization typically 100nm thickness order

- Useful to think it as nearly 2D, semi flat world with some layered structures

Non-location-selective

- Any agitation or process will affect whole surface -> mask material needed
- Alignment between process needed
- Exception: Nano manipulator, Focused Ion Beam



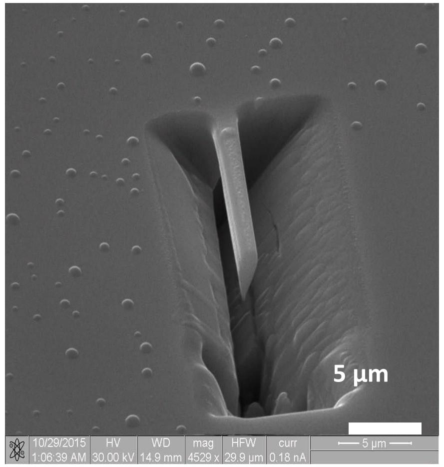
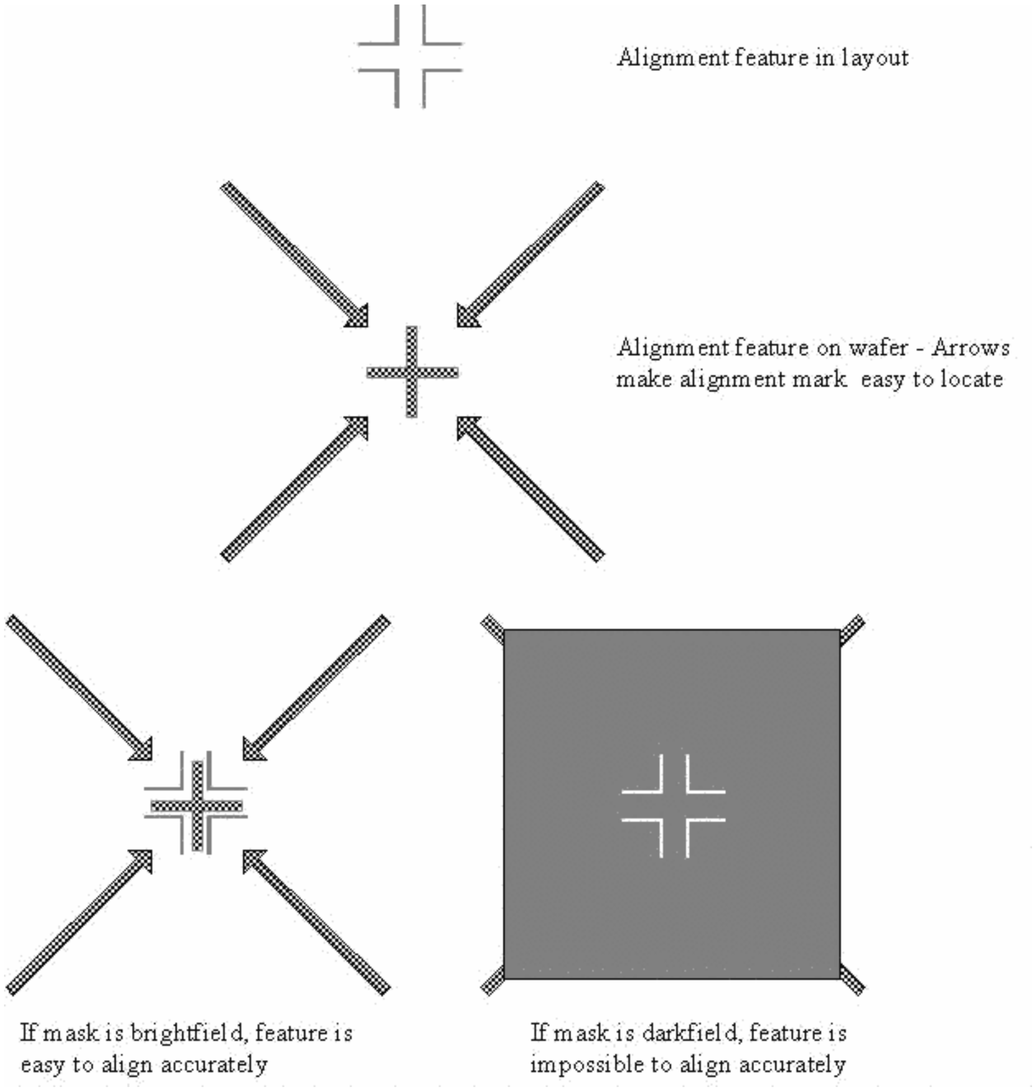
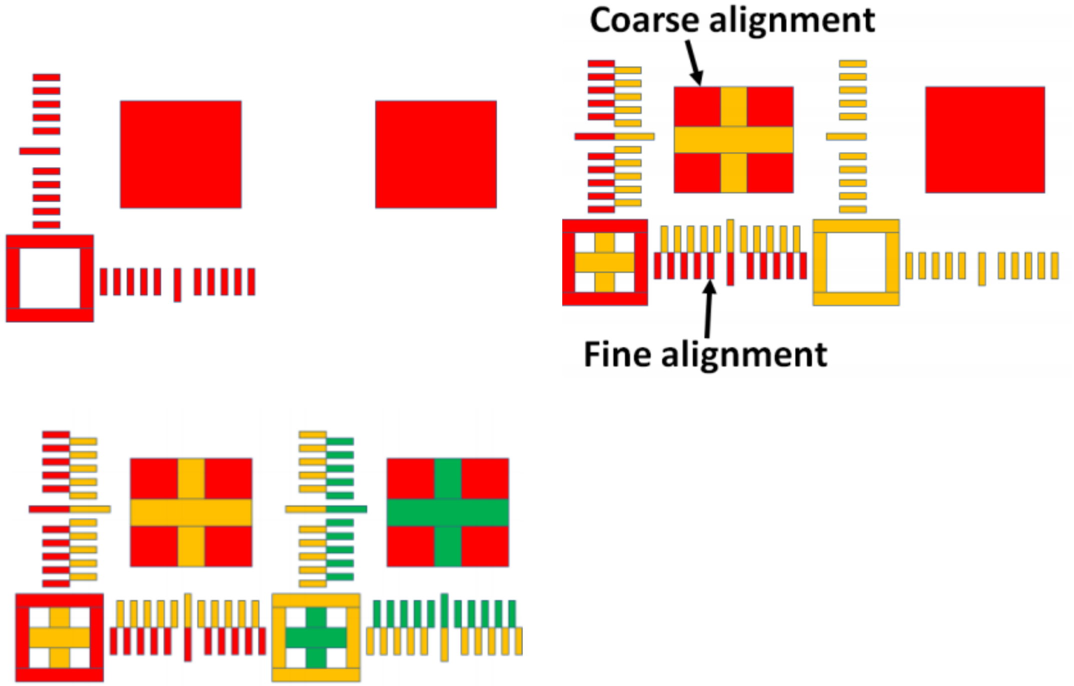


Image: www.nist.gov/news-events/news/2014/05/afm-systems-take-tip-nanowires
From lecturer

Alignment

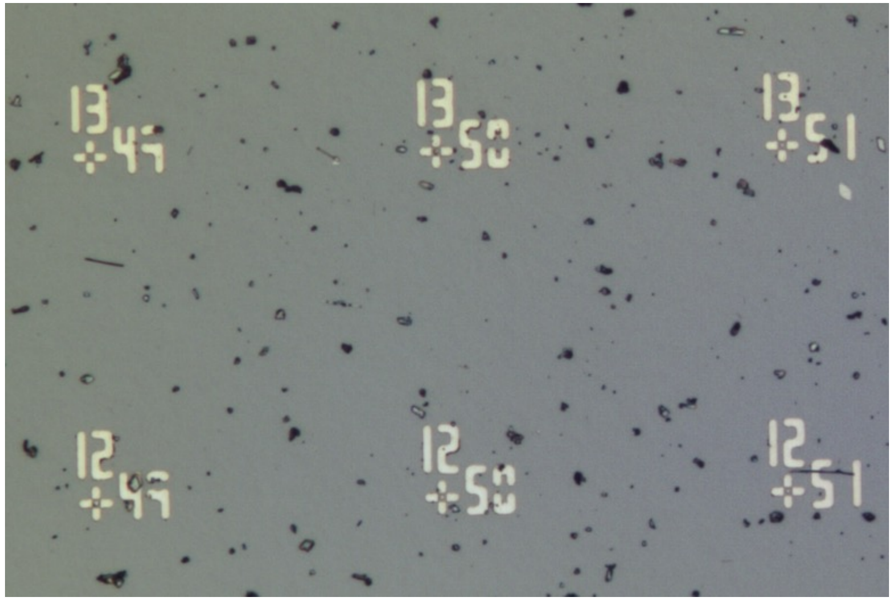




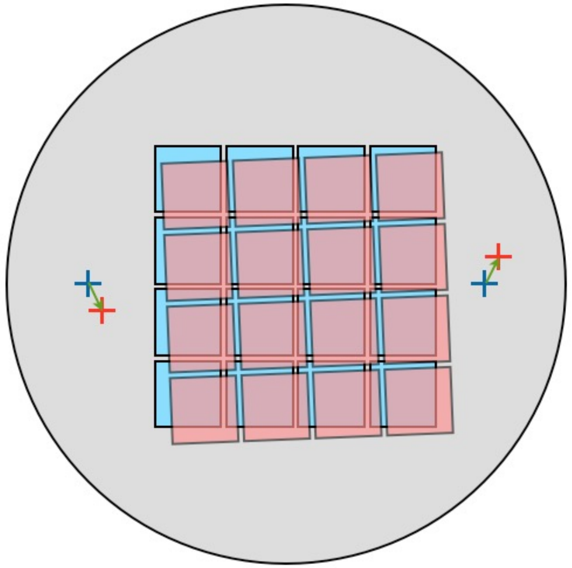
- Vernier Calipers
- Duplicate for multiple steps

https://www.mems-exchange.org/users/masks/intro-equipment.html
NOTES FOR TROUBLESHOOTING ALIGNMENTS By Dr. Yusha Bey

Alignment



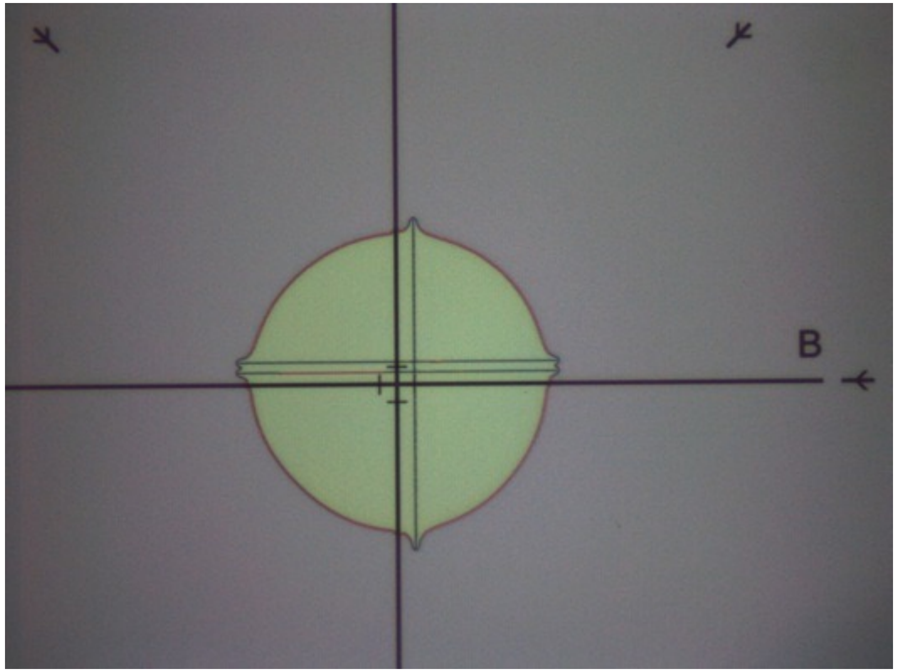
- For EBL: location labeling is handy
- Non- symmetric pattern

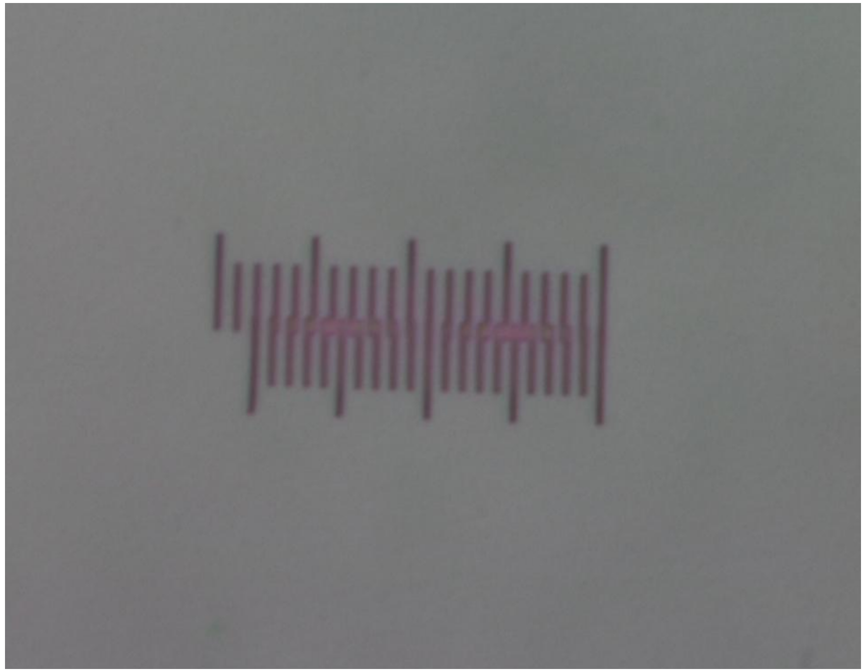


- For angle alignment, large scale alignment is preferable

From lecturer
Https://ebeam.wnf.uw.edu/ebeamweb/doc/jobfiles/align/markdesign.html

Alignment





- In EBL: Seeing is writing
- leave space around each marker

- Modified SEM: for different Beam current & magnification
- => offset correction needed

https://ebeam.wnf.uw.edu/ebeamweb/doc/jobfiles/align/markdesign.html
From lecturer

Drying your sample

- Drying residue, N2 blow
- What medium and contamination
- How to hold your sample
- Tools and jig
- Surface tension: anything that can break?
- Low surface tension liquid
- Critical point dryer

Process integration

- Your decision making = process integration
- Goal: 1) output of process compatible with the next

  2) final device is functional

- Required: fundamental understanding + attention to details
- “whatever can go wrong, will go wrong”
- “Devil is in the details”
- “Assumption is the mother of all mess-ups”

- **Don’t assume Anything**

Process integration

- Familiar with practical details of unit processes
- Understand materials interactions: effect of temperature, chemistry, contamination
- Know the limit of the equipment: manual is not enough, ask questions
- Account for the human factors:

1) People make mistakes

2) Communication errors are common

3) Do not rely on your memory, document everything

4) If allowed have buffer margin in your recipe

Sometimes one image can speak louder than a page long report

Our hypothetical fab facility

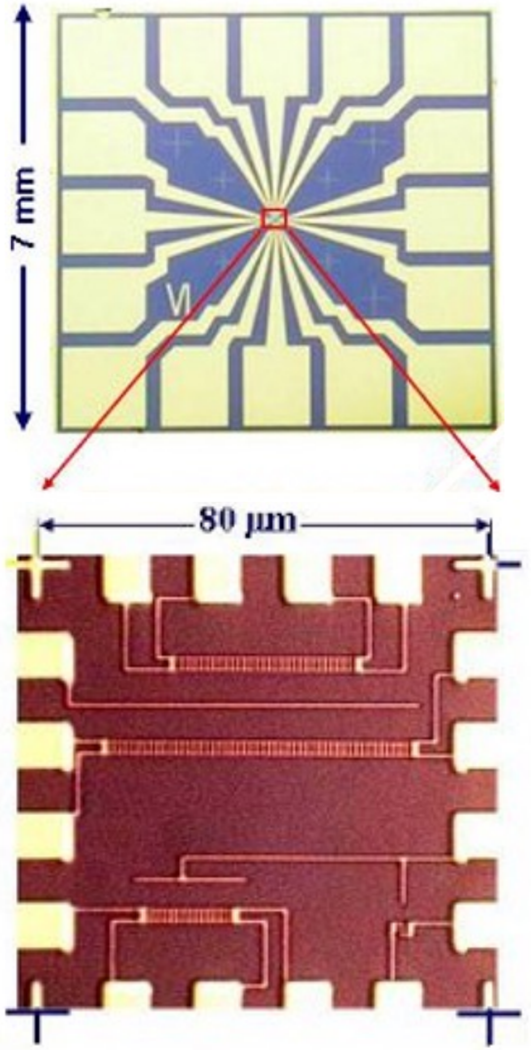
In-house

- E-beam Lithography
- Mask aligner
- Reactive ion etcher
- Oxygen asher
- Spin coater, hot plate, fume hoods
- Critical Point Dryer
- E-beam (or thermal) evaporator
- Sputter
- Wire bonder

Accessible external

- ALD, CVD
- ICP RIE
- XeF2 etcher
- Focused Ion Beam
- Flip chip bonder
- Dicing saw

Case 1: scale matters



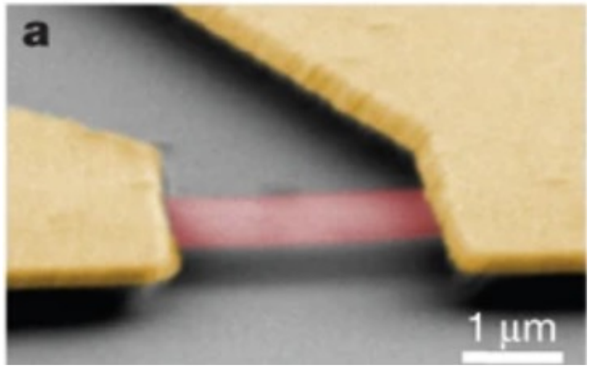
Min linewidth ~500nm

- Supervisor asks you to plan sample fab.
- Photo or e-beam litho?
- Minimum feature? <1um, pitch 1:1
- Your lab mask aligner good for at best 1um

- Mix and match or all e-beam
- Thickness of metal at Pads and small feature

Image: https://www.intechopen.com/chapters/8670

Case 2: Process compatibility

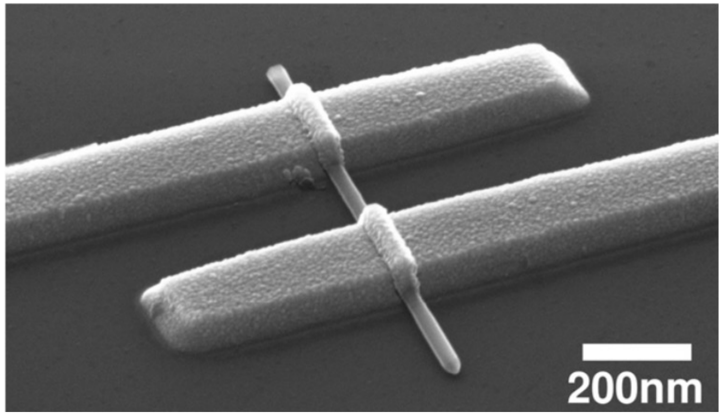


- Want to make suspended graphene devices
- What should be your electrode materials?
- E-beam or photo?
- How to dry?

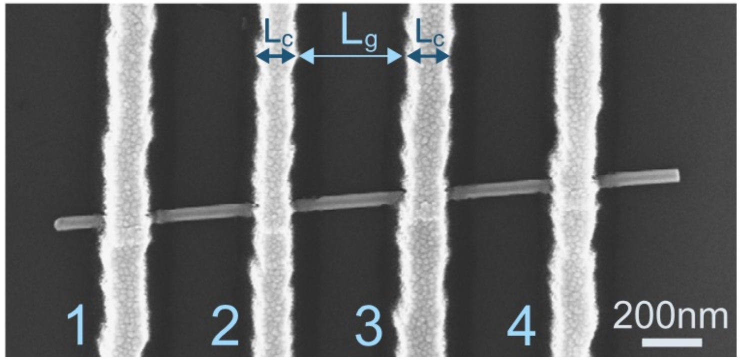
- SiO2 etched with HF
- HF attacks Ti -> Cr/Au
- PMMA is better than photo resist with less residue
- Low surface tension liquid drying or CPD

Image: *Nature* **462**, pages196–199 (2009)

Case 3: making electrical contact



- InAs Nanowire devices for transport measurement
- Native oxide layer lead to contact resistance
- What to do?



- Literature search for contact materials
- Chemical etching: ammonium polysulfide solution ((NH4)2Sx)
- In-situ Ar milling + deposition without breaking vacuum
- 4 probe measurement to verify

Image: *Nanotechnology* 24 045703 (2013)

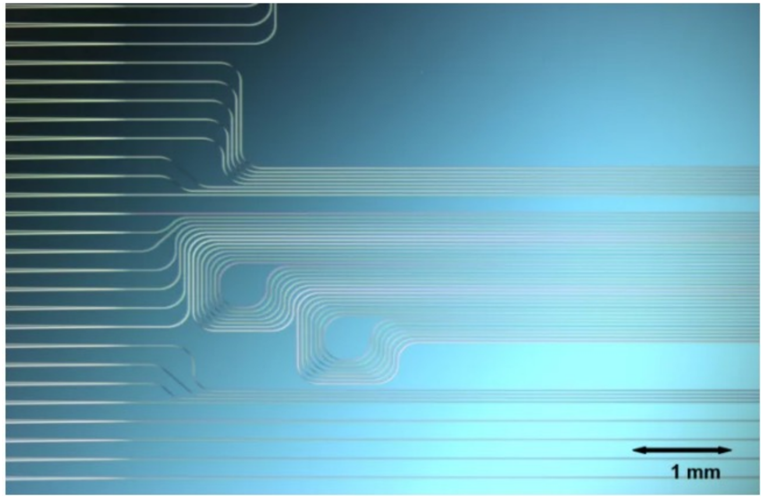
Case 4: e-beam Litho solution

- You are a PI and want to e-beam litho
- Which solution you should look for?
- E-beam Writer (2M USD)?

- EBL machine such as JEOL shines

1) When writing small feature over large scale (nano scale stitching)

2) For high aspect ratio resist pattern (high acc voltage)



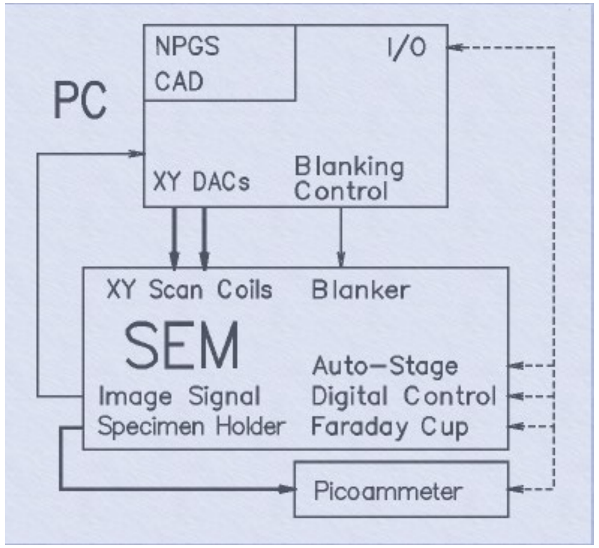
450 nm wide wave guide

Image: JEOL, *https://raith.com/*

Case 4: e-beam Litho solution

- Modified FE-SEM with 3rd party litho, system can be more practical

1) Faster turn around (Job preparation and loading)
2) Could write 10nm with alignment
3) Cost effective

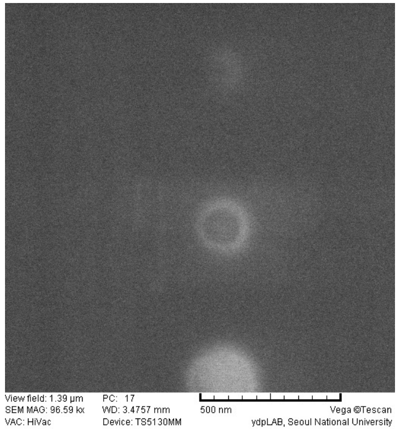


- Nano Pattern Generation System (NPGS)
- Elphy Quantum from RAITH

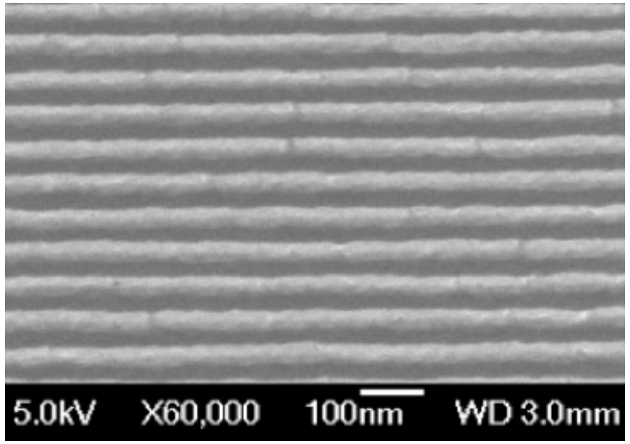
Image: *NPGS website*

Case 4: e-beam Litho solution

- What decide EBL result
- Better machine? Better resist?
- Define what you want: etch mask? Metal Lift off?
- Thinner the resist better the resolution
- Development: temperature, agitation
- Positive resist, negative resist: expiration
- Focus, electro magnetic optics setting: contamination spot



Contamination spot



30nm 1 to 1 pitch lines (with normal Thermal SEM)

Image from lecturer

End of part 1

- Part 2 will be two examples, step by step
- Graphene electronic interferometer
- Superconducting qubit
- And ….. something the most important!

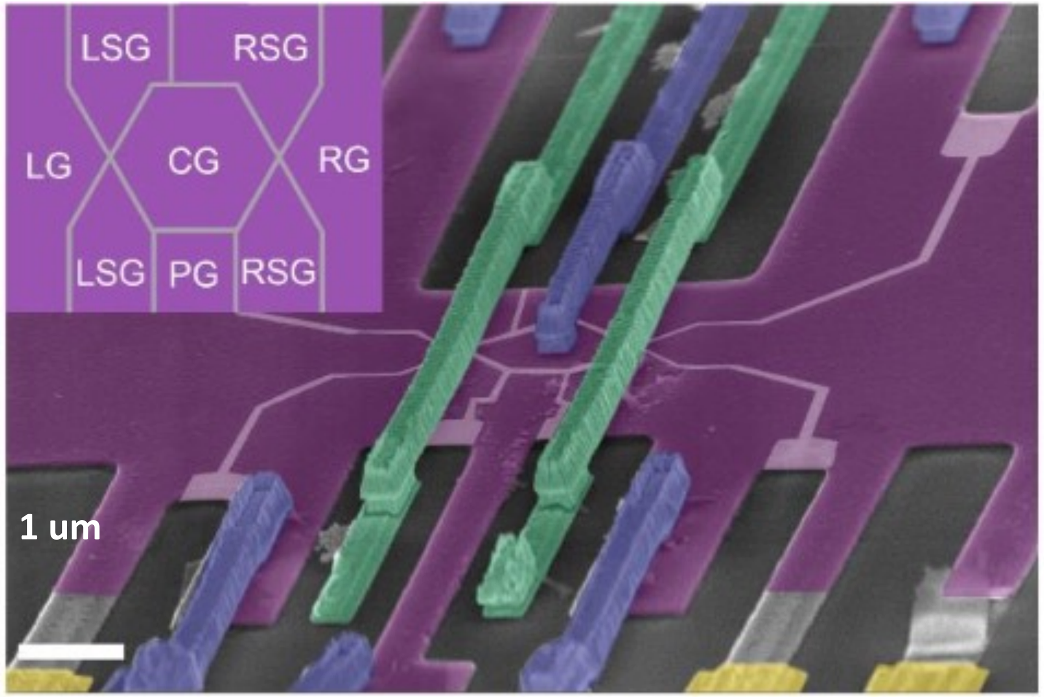
Fabrication Techniques for Quantum Devices

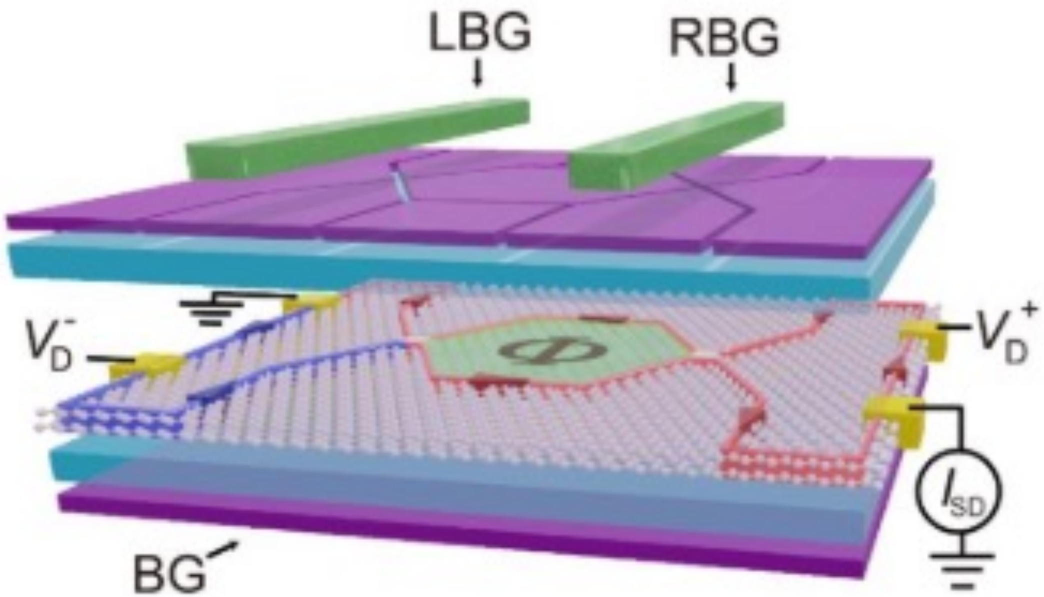
Part 2

The 13th School of Mesoscopic Physics:
Mesoscopic Quantum Devices
23 MAY 2024

Myunglae Jo

Example 1 : Graphene electronic interferometer



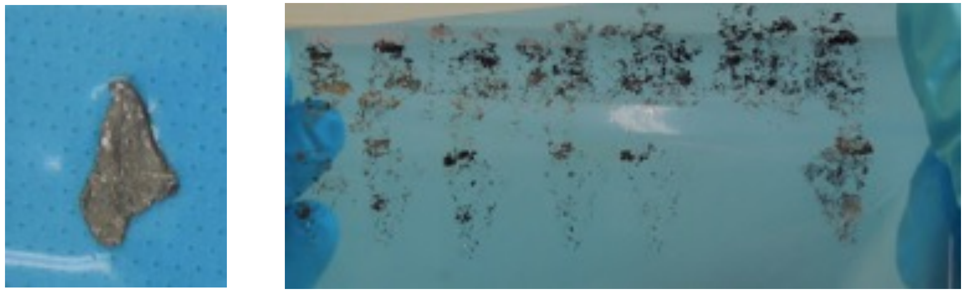


- Yuvan Ronen group’s recent work: FPI for FQHE

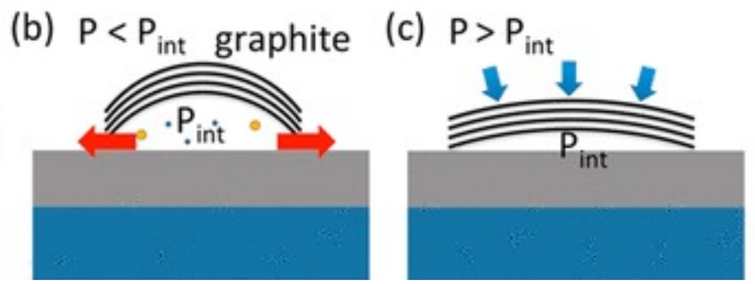
Let’s follow step by step

arXiv:2402.12432

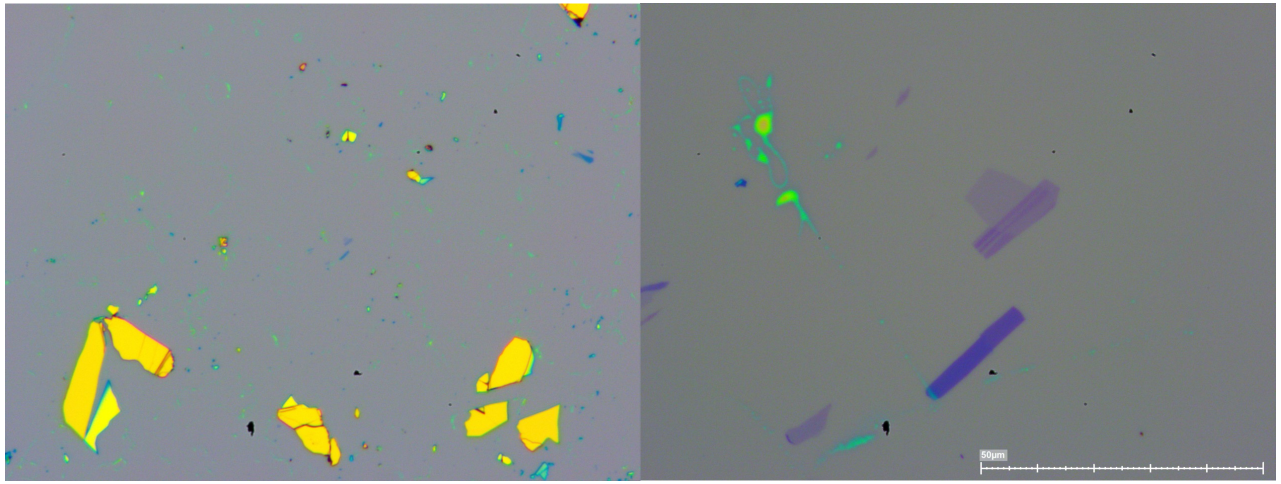
Graphene exfoliation



Mechanically exfoliated (blue tape) [1]



170C heat and cool [2]

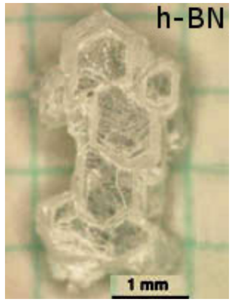


- Visually select
- AFM, Raman
- Highly trained eyes: >95% (single layer)
- Image contrast and polarizer to spot unseen defects

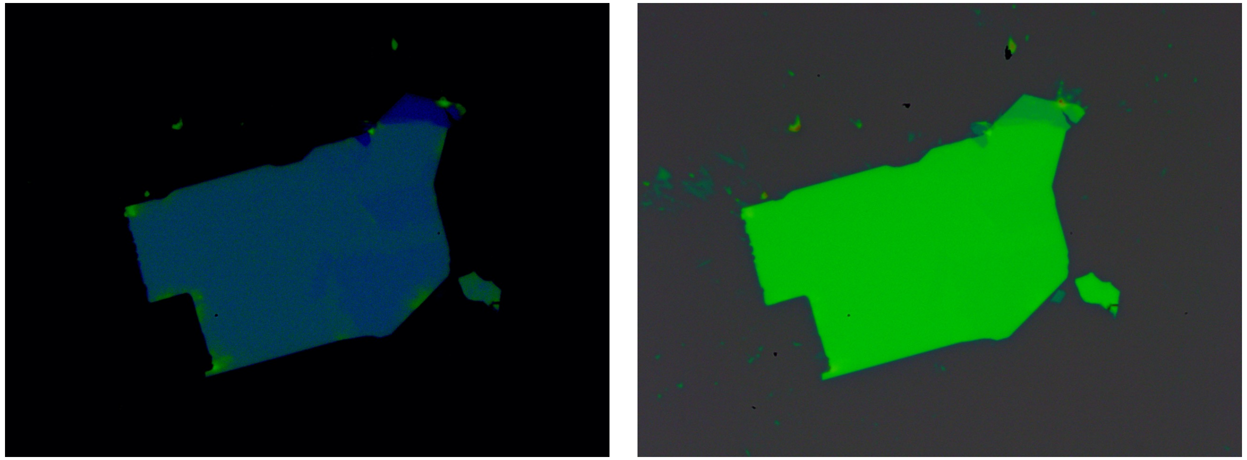
[1] Thesis, Graphene Resonators with High Quality Factor Using a Substrate Independent Transfer Technique

[2] ACS Nano 2015, 9, 11, 10612–10620

hBN exfoliation

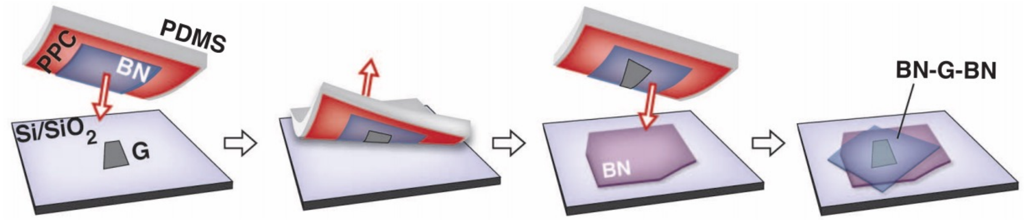


- Kenji Watanabe and Takashi Taniguchi
- -> hBN from NIMS
- Exfoliated on PDMS (gel Pak)
- On to SiO2/Si and 80C heat and cool
- Slow peeling



- Image contrast and polarizer to spot unseen defects
- Choose suitable thickness by colour chart and AFM
- Limitation can come from size and uniformity of hBN not by graphene

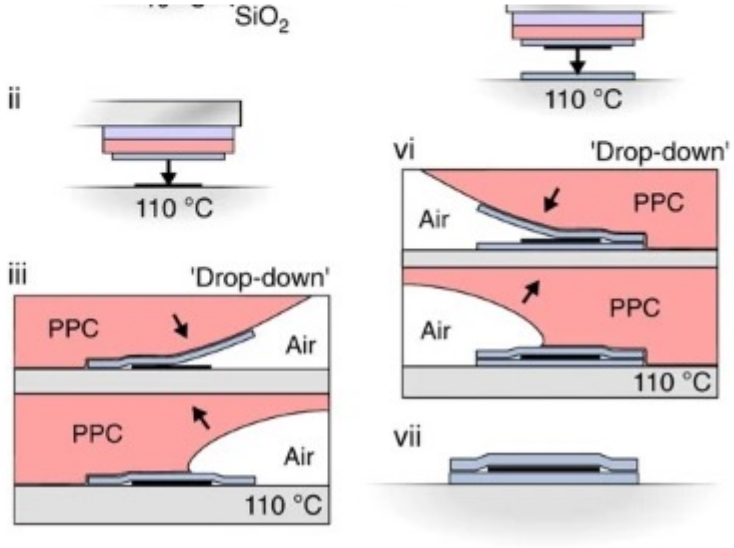
Dry transfer, stacking

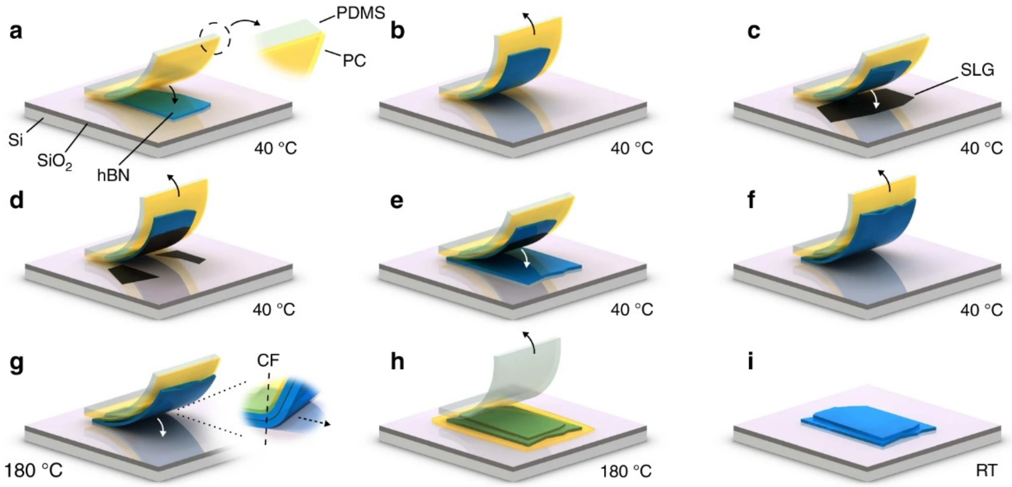


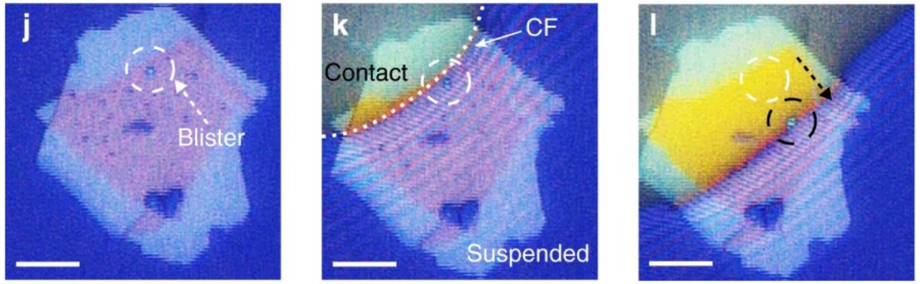
- PC(sticky layer) film hold by Kapton tape on PDMS (cushion)
- PC stamp pre-run
- 130C hot pick technique
- Top graphite (12nm)-> top hBN (48nm) -> bilayer graphene-> bottom hBN (32nm)-> bottom graphite (6nm)
- Landed on clean substrate at 180C, melt PC and leave stack on the substrate

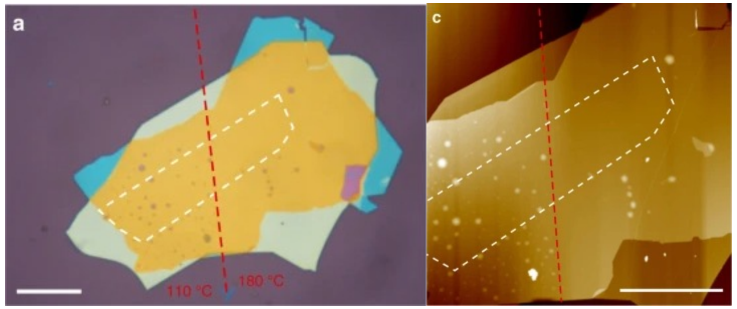
From CEA

Hot pick up







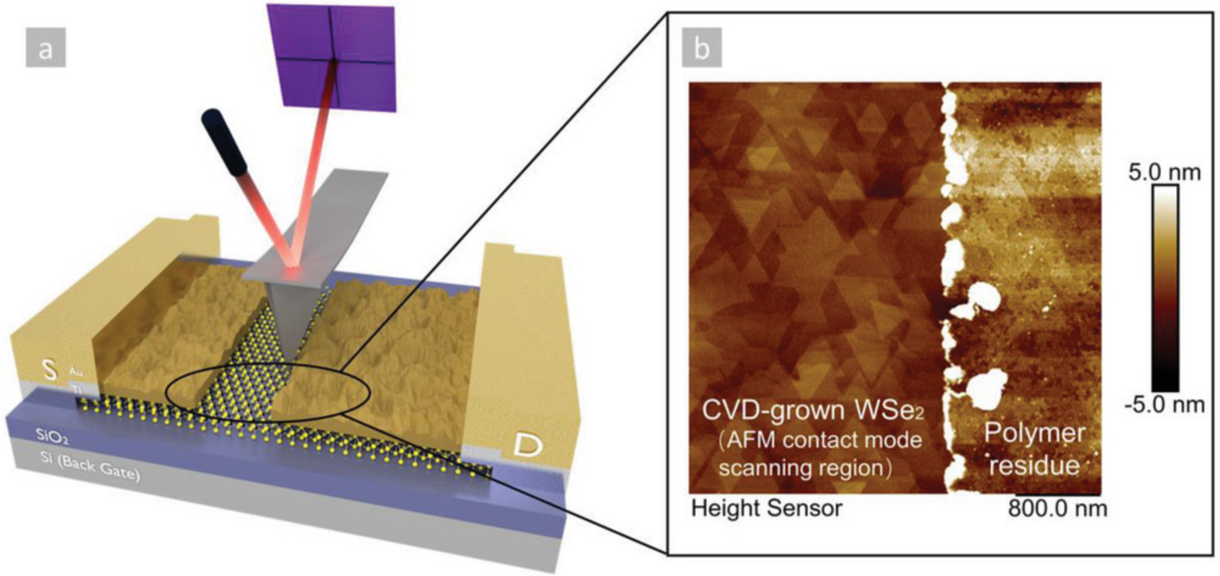


- Contaminant more mobile

Nature Communications 7, 11894 (2016)
Nature Communications 9, 5387 (2018)

Treatment after stacking

- Melt PC removed with Chloroform -> IPA > DI
- Thermal annealing with UHV (10^{-9}Torr) at 400C 4hrs
- Annealing remove leftover residue and bubbles.
- AFM cleaning



Advanced Materials Interfaces 6, 1801321 (2019)

Sample process 1

Prepared stack

E-beam litho: Align mark,

bonding pads

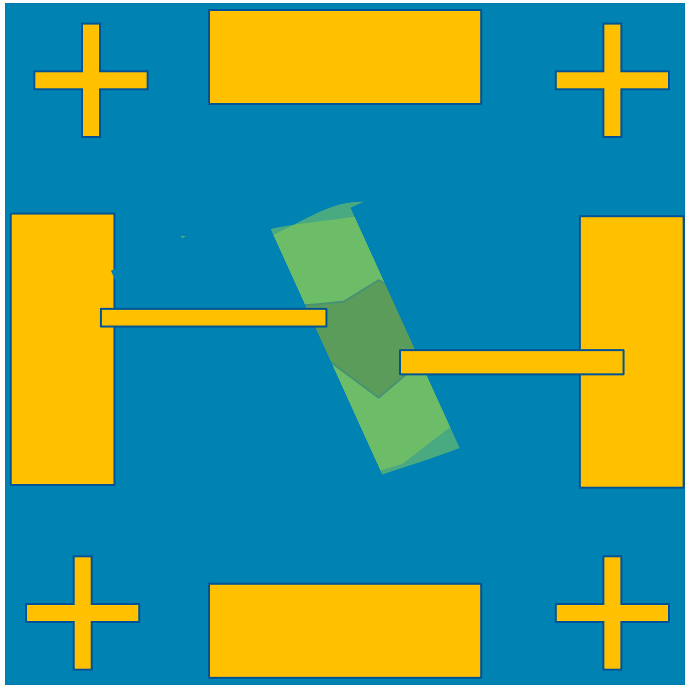
Ti 10/Au 60/ Pd 20nm

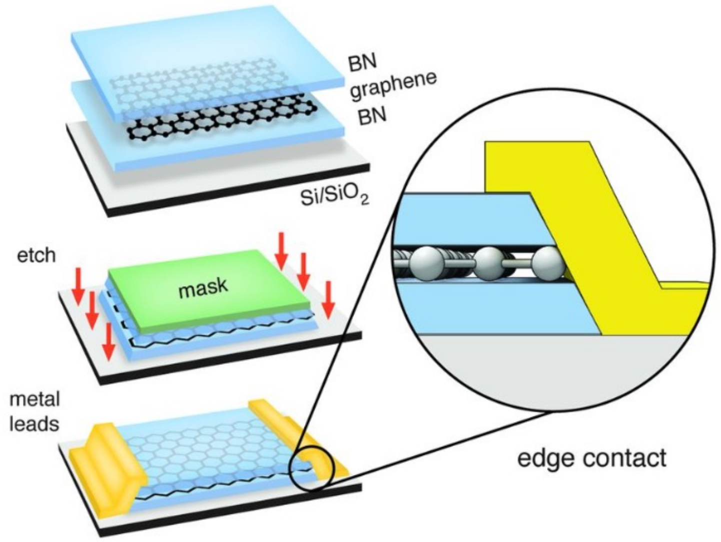
E-beam litho: PMMA as mask, RIE etch

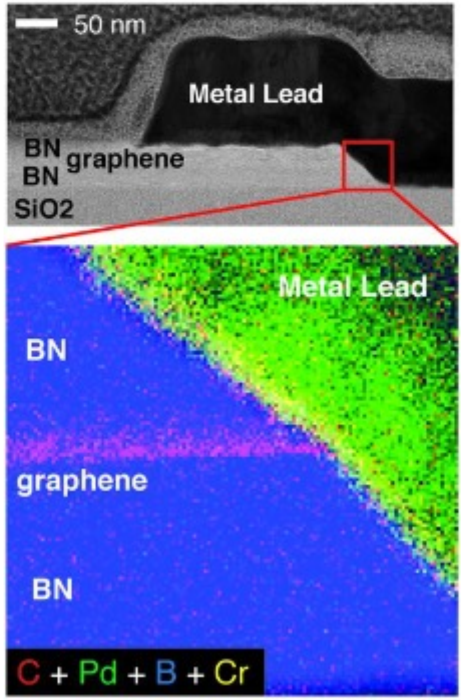
O_2: graphite, O_2 /CHF3 :hbN

Annealing UHV (10^{-9}Torr) at 350C 2hrs

Sample process 2







E-beam litho: PMMA as mask,

etch top hBN + metallization

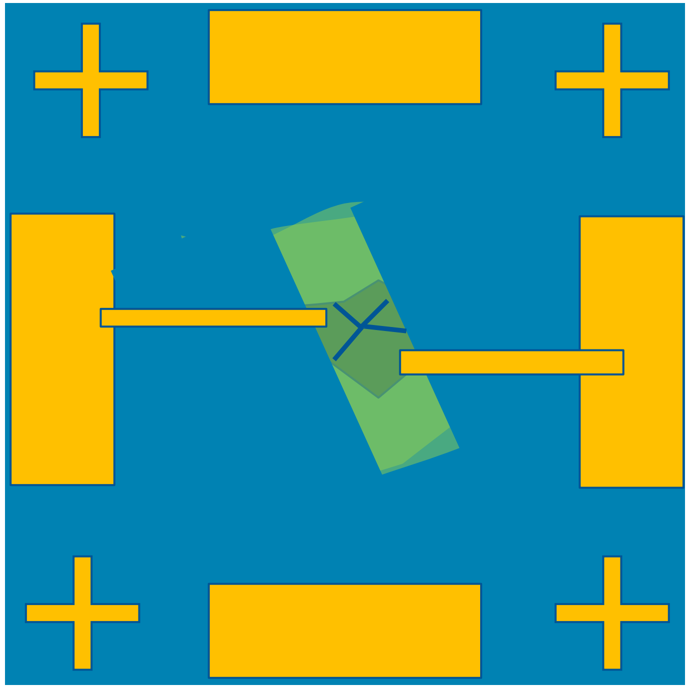
Cr2/ Pd 13/ Au60 nm tilted

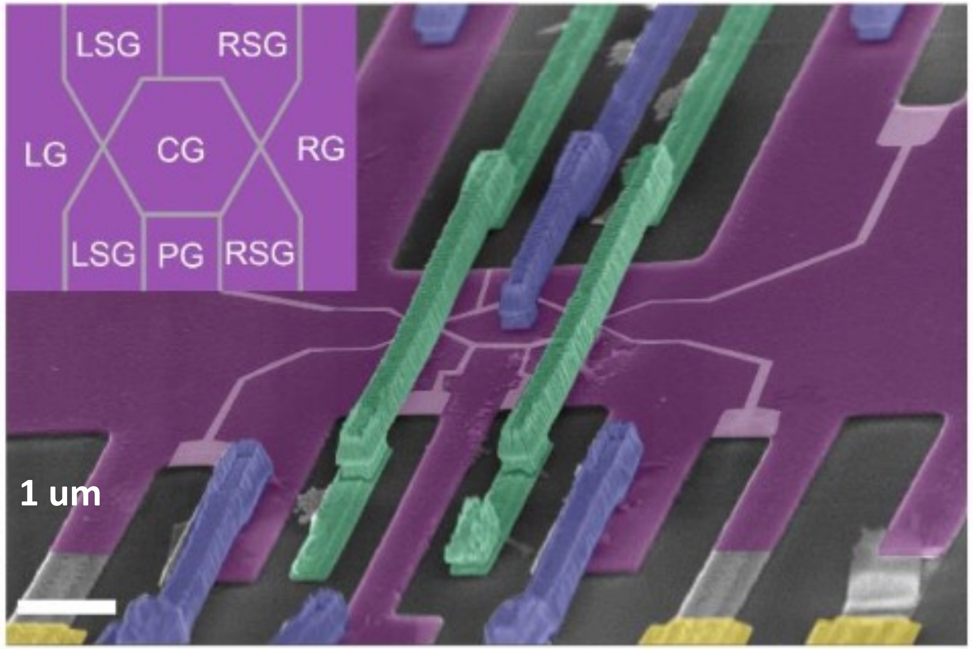
Edge 1D contact

Cr, Pd: good work function match with graphene

SCIENCE (2013) 342, Issue 6158 pp. 614-617

Sample process 3



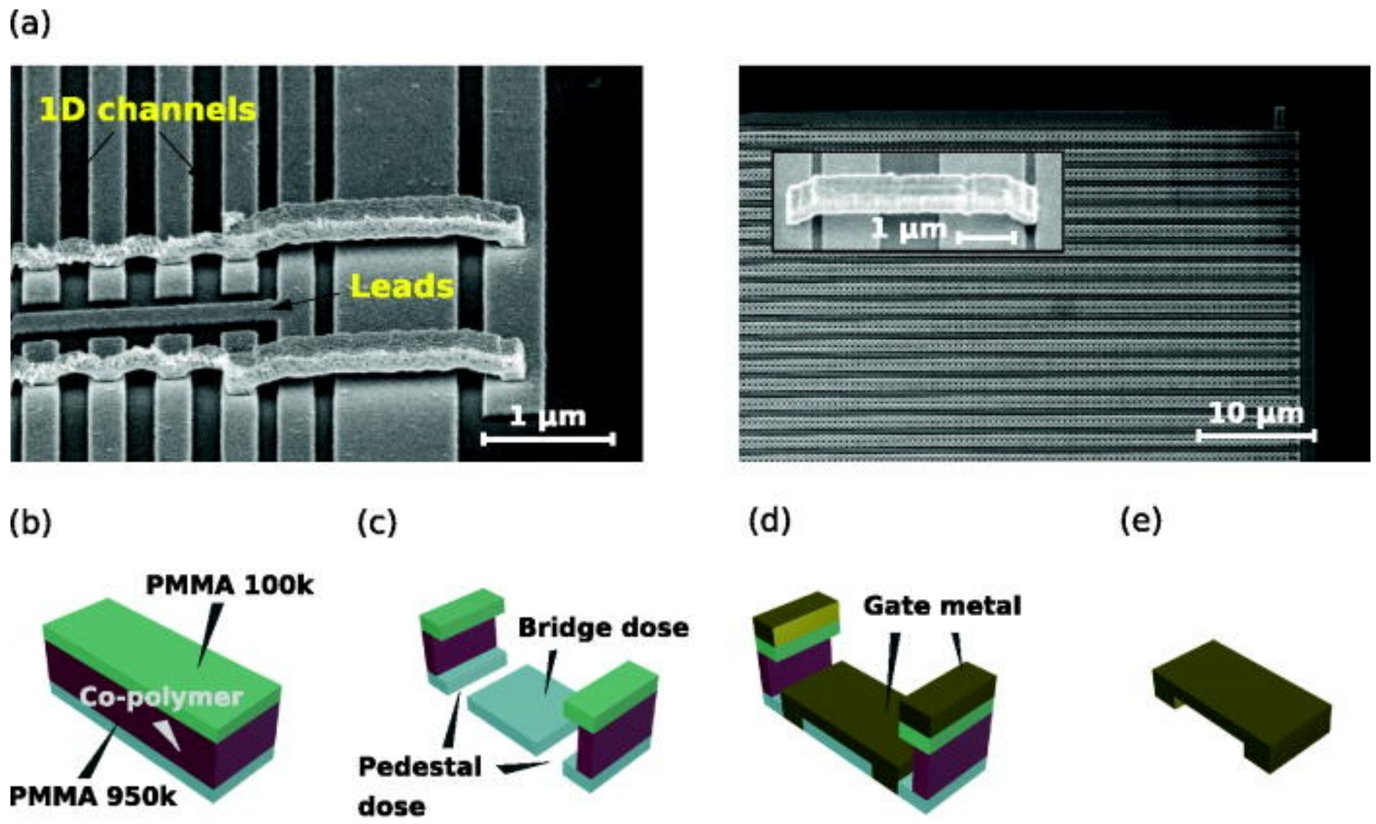


E-beam litho: 40nm trench on graphite, O_2 RIE

E-beam litho: air bridge using PMMA/MMA/PMMA -> O_2 plasma -> Cr 25/ Au 320nm

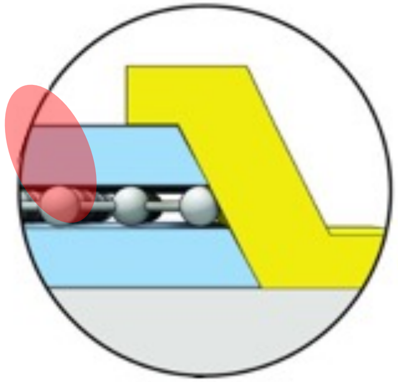
Air bridge

- Air bridge using PMMA/MMA/PMMA ?
- MMA dose < PMMA
- 100K PMMA dose < 950K PMMA dose
- Thick metal for mechanical stability.
- 0 deg deposition for better lift off
- Probably no sonication
- moreover 2D stack and sonication are not friendly
- Top 950K PMMA for better lift off



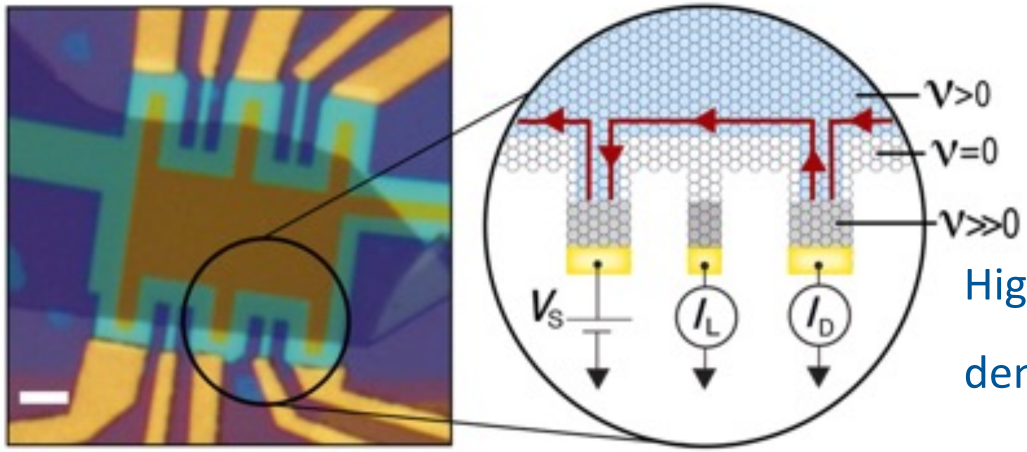
Appl. Phys. Lett. 118, 162108 (2021)

Doping of the contact



Unwanted doping

Reduced transparency

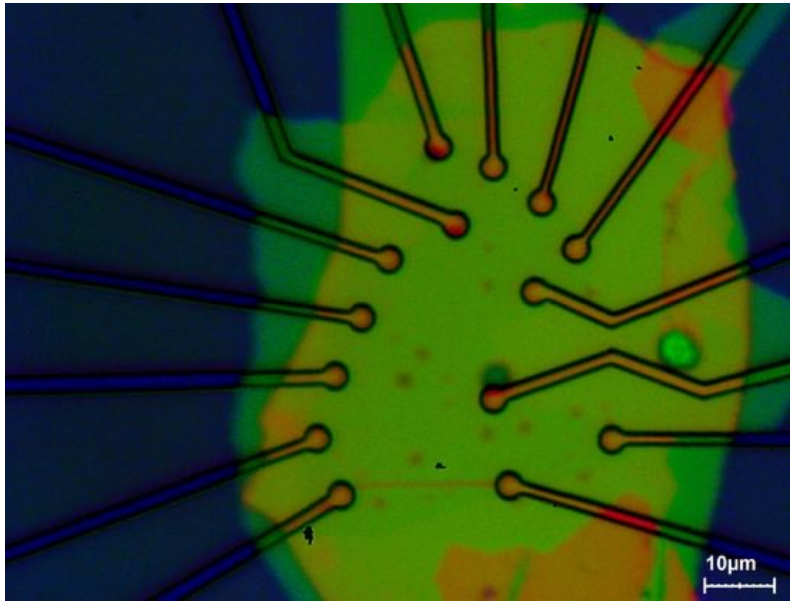


Higher carrier density

- In this sample, heavily doped Si with 280nm oxide was chosen
- Si gate will push extended graphene touching metal contact to metallic state

Nano Lett. 19, 2583–2587 (2019)

Unwanted crack during development



- Although PMMA has very good adhesion nature
- Issue with hBN: crack after development
- Crack = stress + medium + initiation defect
- MIBK developer: PMMA swelling during development > stress
- Using cold temp IPA+DI as developer: lowering stress [1]
- Or gentle oxygen plasma treatment

- Although effect of Oxygen plasma seems not permanent
- It is known that extensive oxygen plasma can etch hBN

[1] Nano Lett. 17, 5389–5393 (2017)

Charging effect

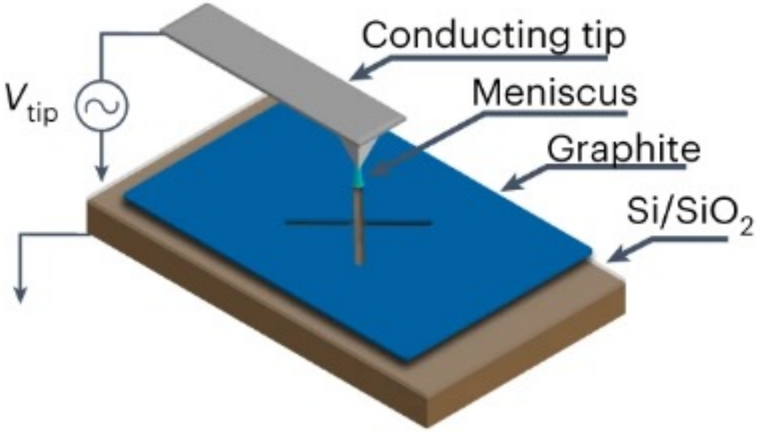
- Interestingly charging effect has been shown on top of hBN region
- Anti charging remedy should be used: Acc voltage, anti charging coating, dose compensation

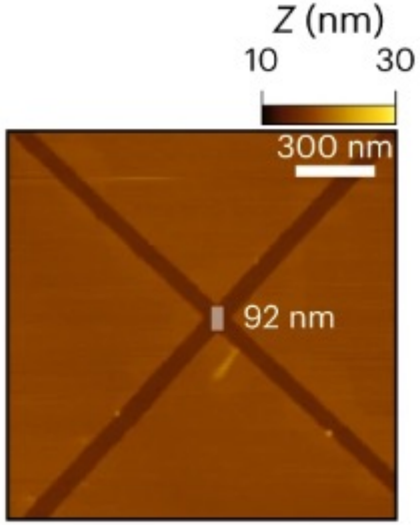
Cleaning PC residue

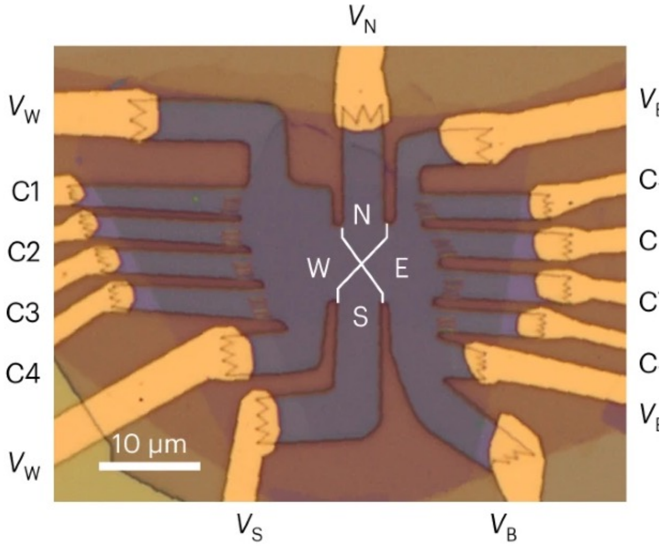
- Sometimes annealing is not permitted: ohmic contact degradation, magic angle graphene
- Strong solvent can be used with limitation: Chloroform …

AFM as lithography machine

- To make very narrow gap in the graphite
- local anodic oxidation or mechanical scratch

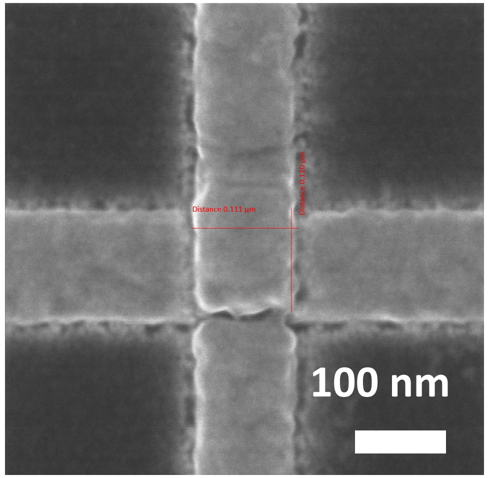


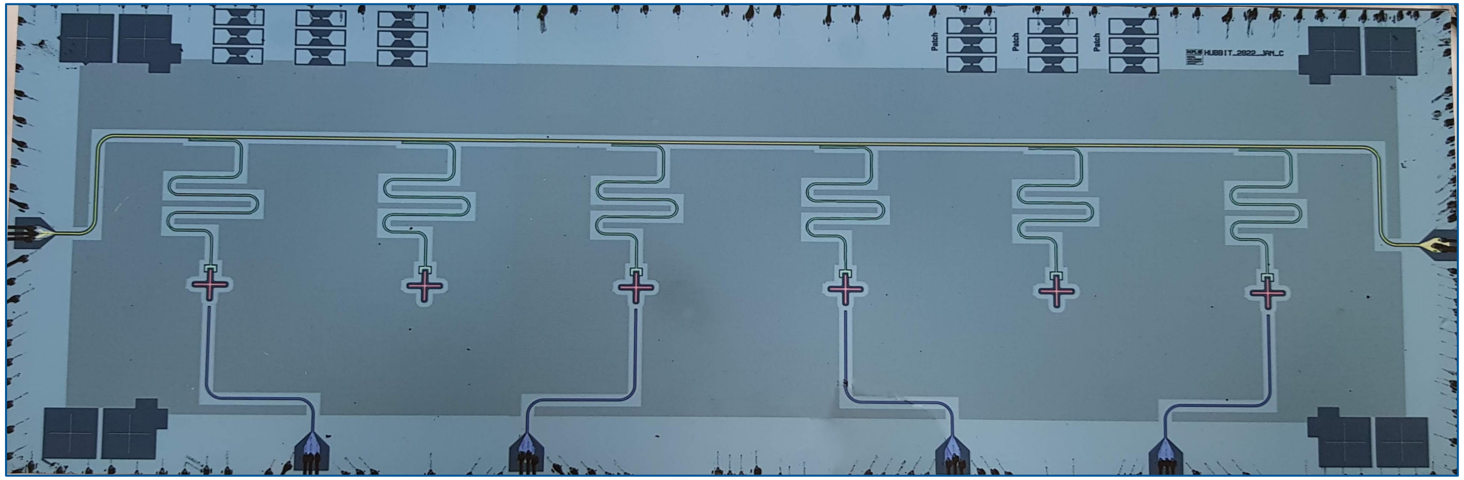




Nature Physics 19, 1502–1508 (2023)

Example 2 : Superconducting qubit





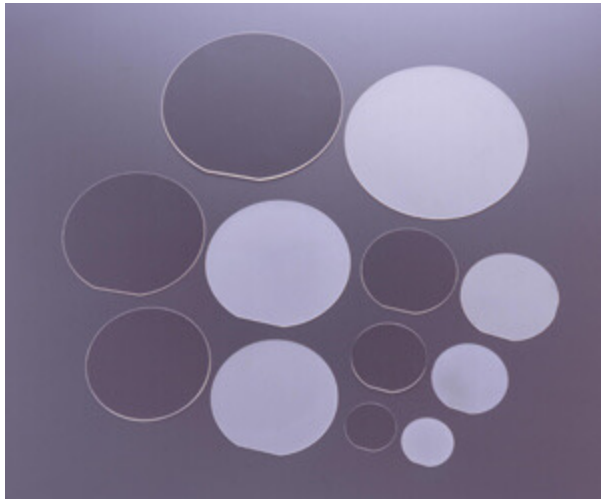
- SC qubit = Josephson junction + metallic RF circuit

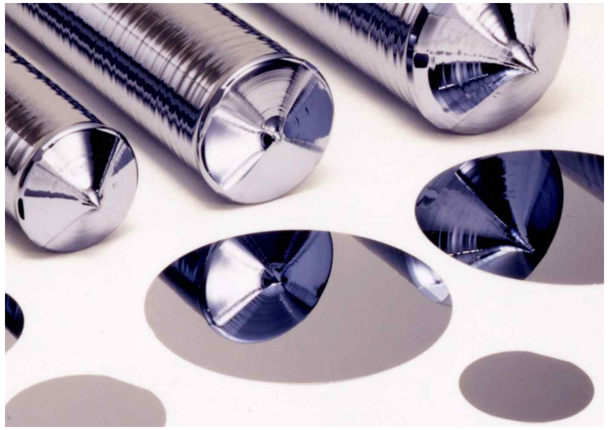
Let’s follow step by step

From lecturer

Choice of wafer

- Dielectric properties, Loss tangent
- Sapphire widely used
- But expensive, anti charge coating etc.
- Recently Intrinsic Silicon favoured
- Accessible, EBL friendly, process well known etc.





Precleaning

- Piranha solution 3min 65C, DI rinse -> hydrophilic
- 2.5% HF dip 5min, DI rinse -> remove native oxide-> hydrophobic
- Load the wafer in the evaporator ASAP typically 5min
- Pump out the chamber 5e-6mbar -> heating up to 700C, hold 30min then cool

- Whole purpose is the interface between Al and Si as pristine as possible

1st Al layer evaporation

- Pump down to 7e-8mbar (overnight): cleaner the lower TLS
- Pre-deposition (sample shutter closed)
- 0.5nm/s 100nm Al deposited
- 10mbar static oxidation 5min (controlled and saturated)

E-beam evaporator and superconducting QC

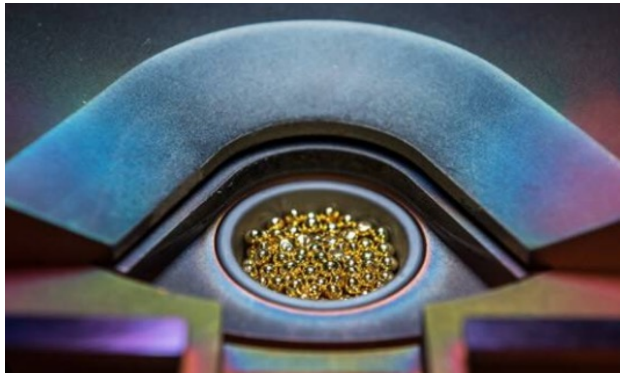
Molten metal is inside 'crucible'

- Crucible materials: high temperature stable, W, Graphite, BN, Al2O3, Quartz, Ta, Mo,

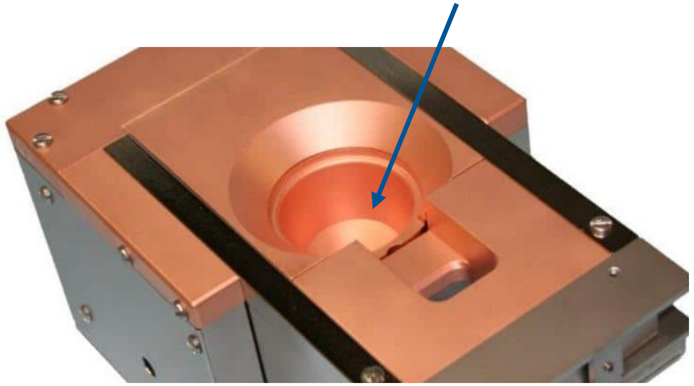
- After >30 years, still natural oxide from Al is the best materials to form highly coherent time qubit
- But High temp Al reacts with many materials and becomes less pure!
- Crucible itself can be problem!

E-beam evaporator and superconducting QC

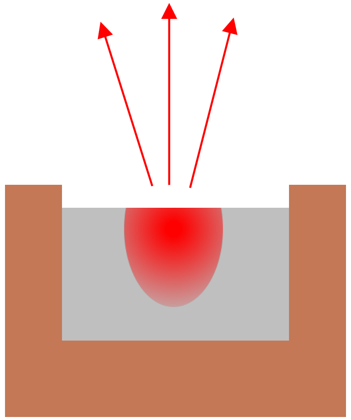
- Solution: using Al as “self limited container”



- Normal use

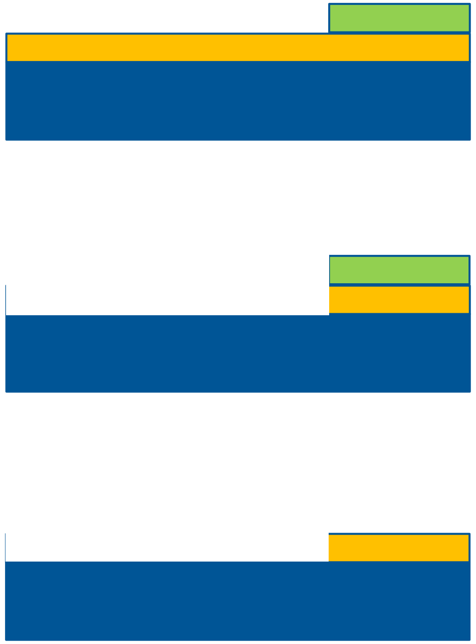


- Copper color part= water cooled crucible pocket, put Al directly in the pocket

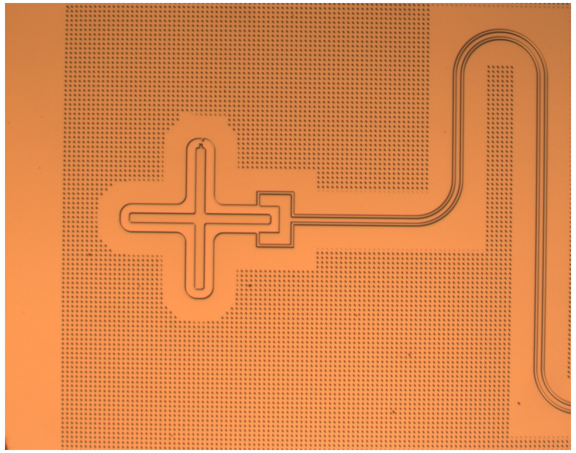


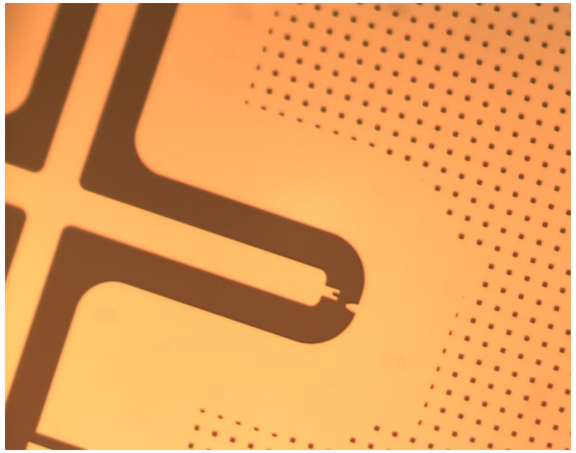
- Due to high temperature difference, only the centre Al melts -> evaporate, while Al touching the copper pocket is remain lower temperature, effectively acting as its own crucible.

1st EBL: Waveguide define



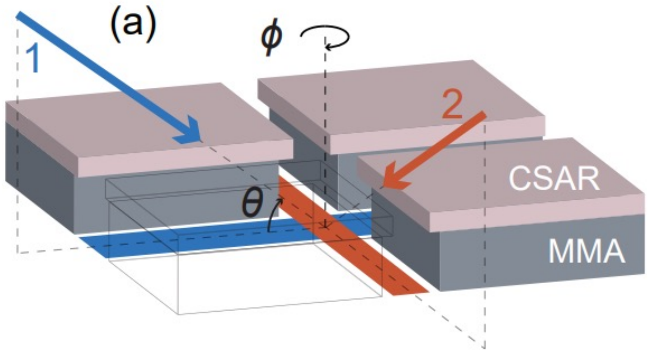
- CSAR 62 resist ~ 600nm
- EBL with JEOL JBX-8100FS, intermediate spot size (100nA)
- Development, descum ashing,
- Bake 5min 160C, promote better adhesion
- Wet etch Al 100nm using EBL pattern as a mask, using photoresist developer, TMAH)
- Remove etch mask with AR600-71 remover





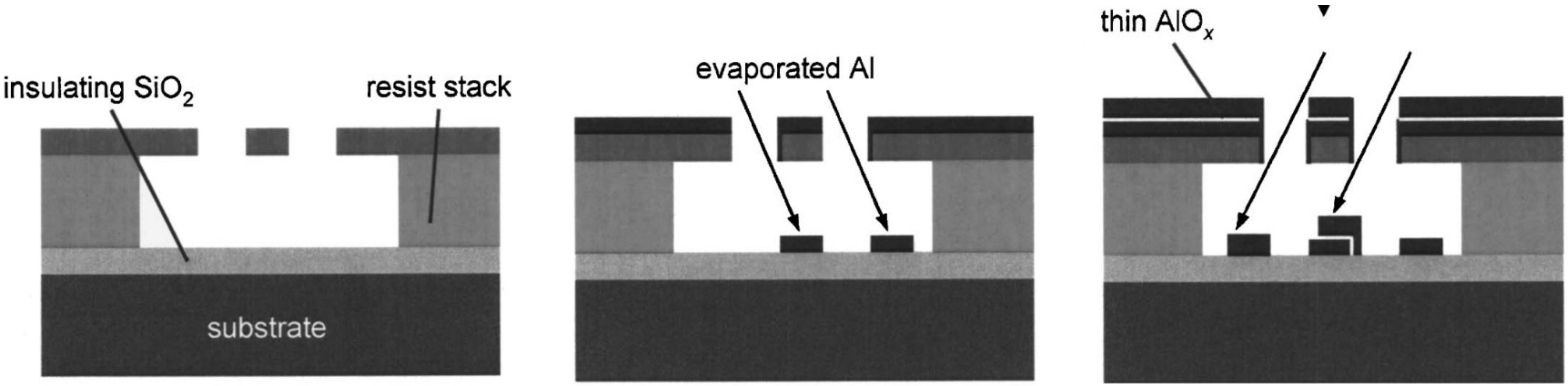
2nd EBL: JJ define

- Copolymer/CSAR 62 double layer, EBL fine spot size (2nA)
- Development top and bottom separately: undercut control
- Descum -> evaporator-> good vacuum
- 30nm angle 45deg -> static oxidation -> planar rotation 90deg
- 45nm angle 45deg -> capping oxidation
- Lift off, with controlled temp and sonic agitation

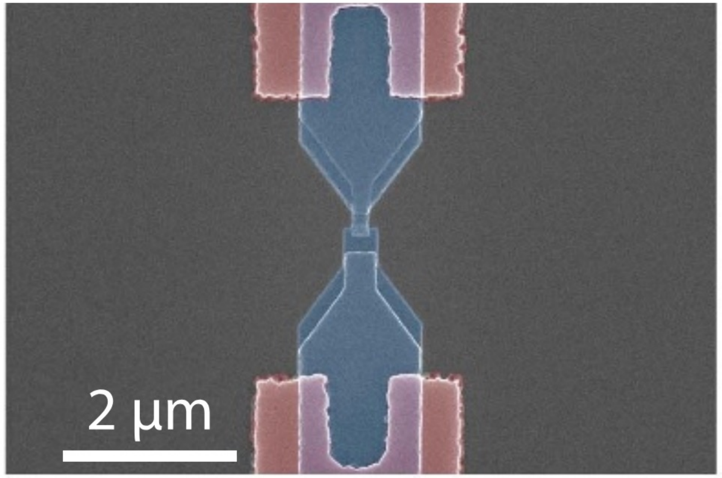


Manhattan style

Dolan bridge



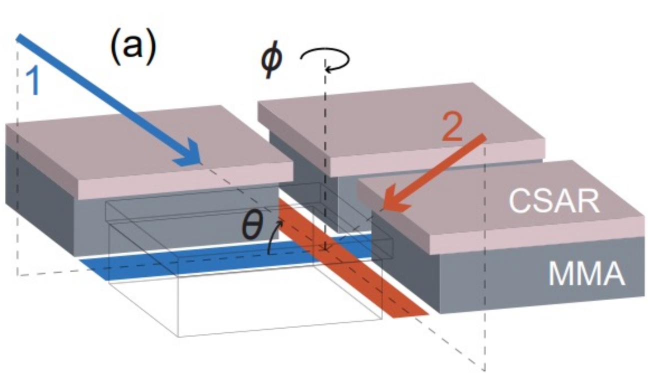
Dolan-bridge junction



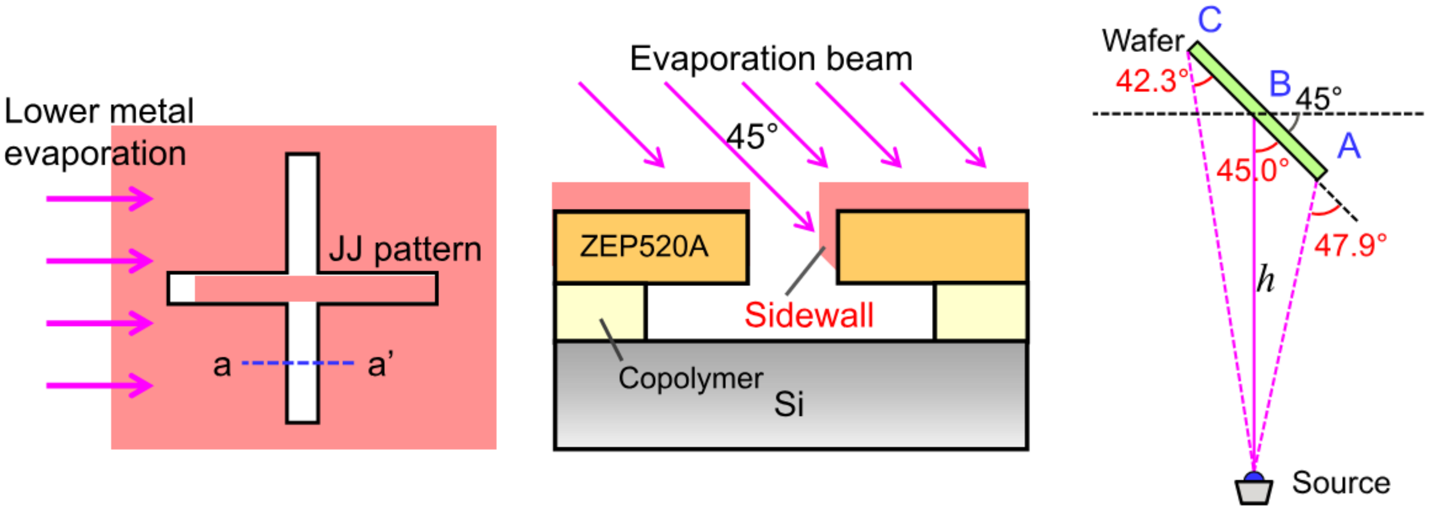
- One angle manipulation (no planar rotation)
- Spurious twin
- Sensitive to resist-height variation (TSV?)

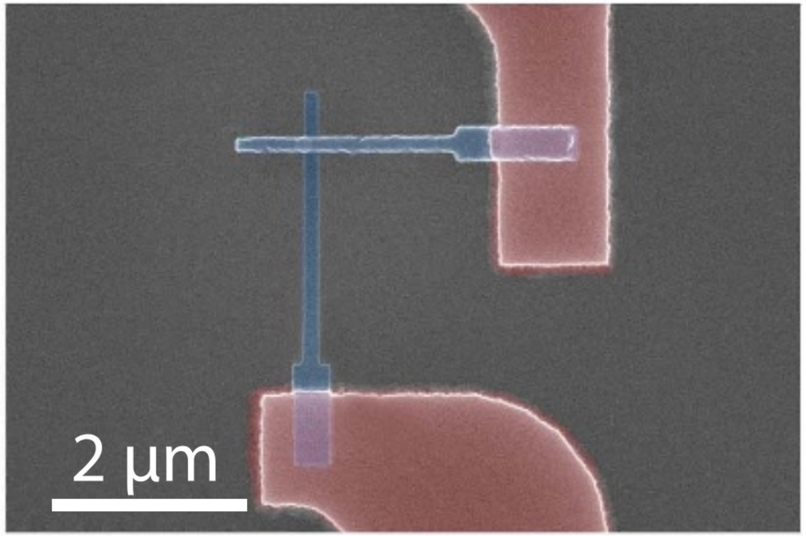
J. Vac. Sci. Technol. B 24, 3139–3143 (2006)
Quantum Sci. Technol. 9 025006 (2024)

Manhattan style



Manhattan style



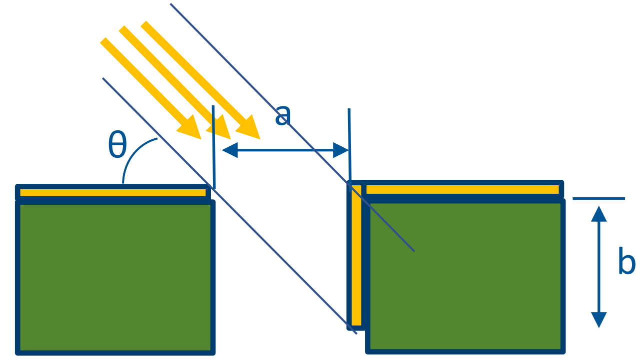


- 2 angle manipulation (tilt and planar rotation)
- Wafer to edge variation
- Narrowing of mask opening by deposition

Jpn. J. Appl. Phys. 62, SC1002 (2023)
Quantum Sci. Technol. 9 025006 (2024)

Undercut Bilayer resist

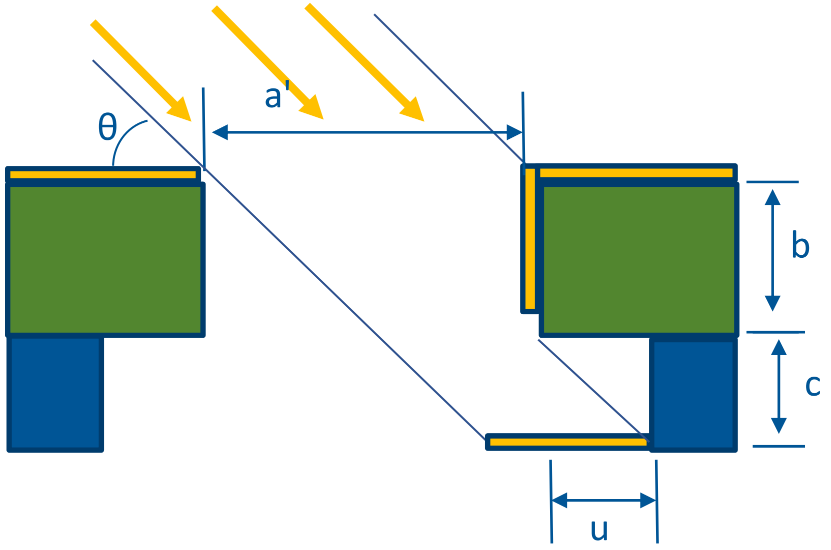
Orthogonal to narrow arm (when you don't get deposition)



Any resist thicker than a(tanθ) can do the job.
For θ=45deg, any b>a

So for 100nm x 100nm cross Junction needs a resist thicker than 100nm

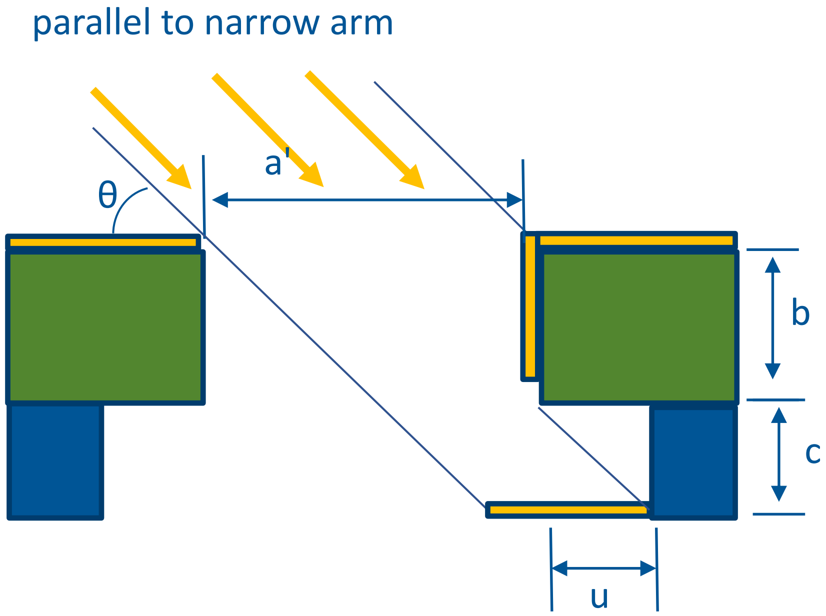
parallel to narrow arm (when you get deposition)



Undercut layer is there for good lift off.
Minimum condition of undercut for no 'bunny ears'
u>c

Why use 700nm bottom layer?

Undercut Bilayer resist



Why use 700nm bottom layer? Probably better undercut?

Others case, UC Berkely, https://doi.org/10.1088/1361-6668/ab8617

C=500nm, b=150nm, θ=45, Al thick= 30,40nm
Undercut was not specified, but from figure 1(b), I could deduce no more than 450nm

Preference of CSAR (or ZEP) over '**PMMA because of the flexibility it offered having (mostly) orthogonal development chemistry to MMA and over ZEP because of its lower cost**'

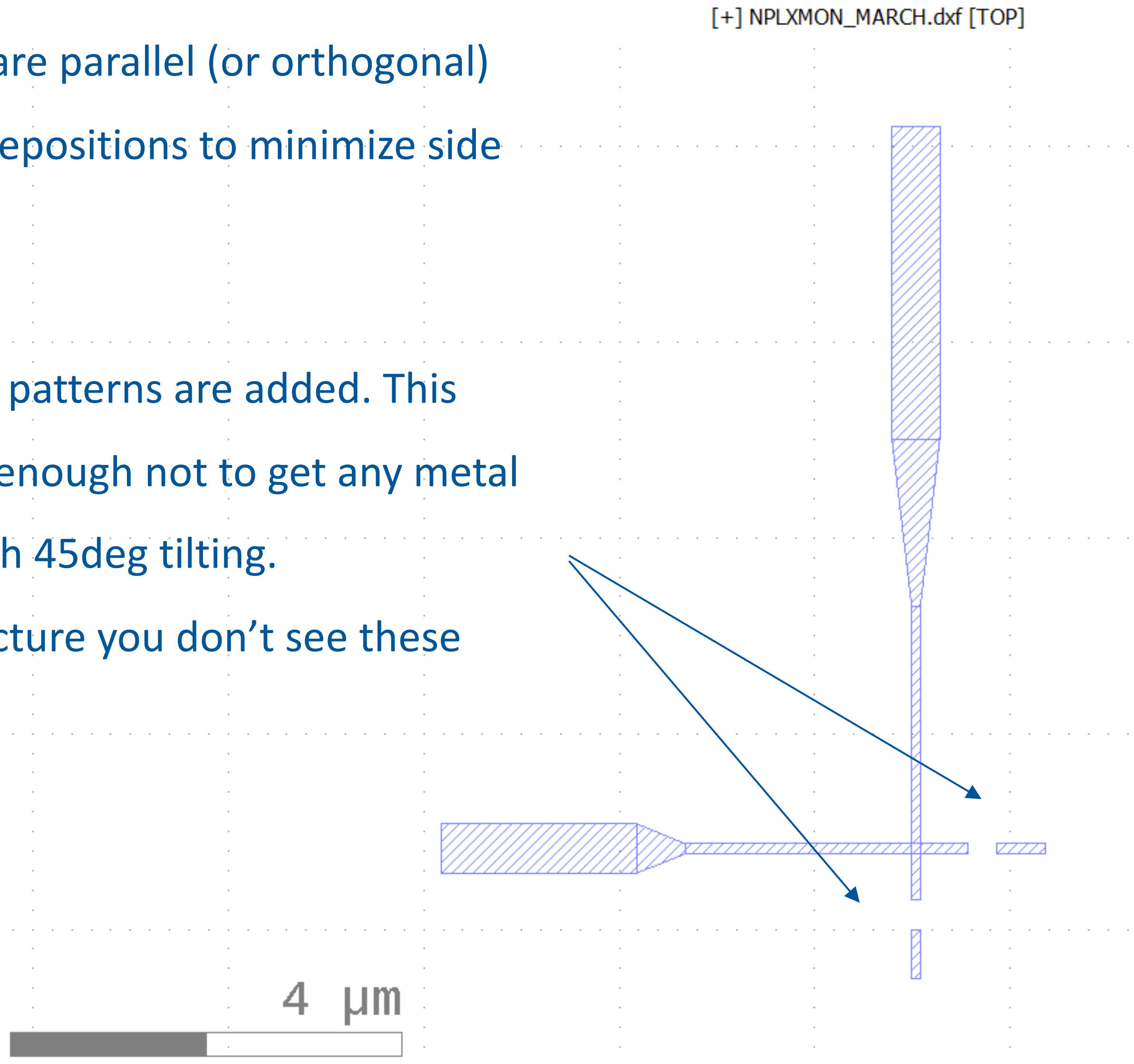
Using IPA+water solution for development of MMA
'**IPA:H2O was a superior developer, resulting in reduced swelling**'

More detailed information see for page 43 and 63 in this thesis from UC Berkely https://escholarship.org/content/qt3gg7j6rh/qt3gg7j6rh.pdf.

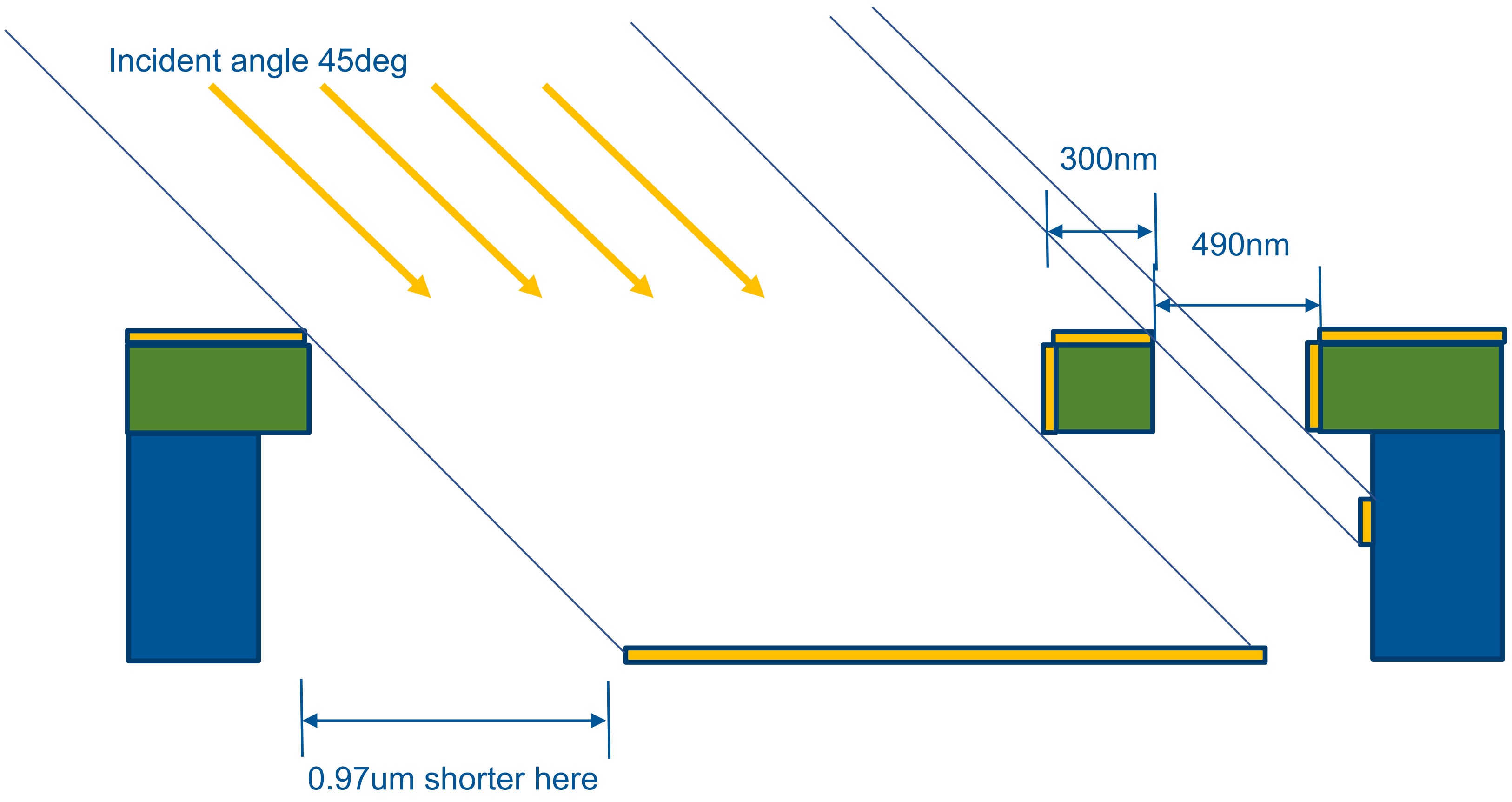
Avoiding side wall deposition

First, every patterns are parallel (or orthogonal) to the directions of depositions to minimize side walling

Additional island like patterns are added. This patterns are narrow enough not to get any metal deposition inside with 45deg tilting.
So in the final JJ structure you don’t see these island.



Avoiding side wall deposition



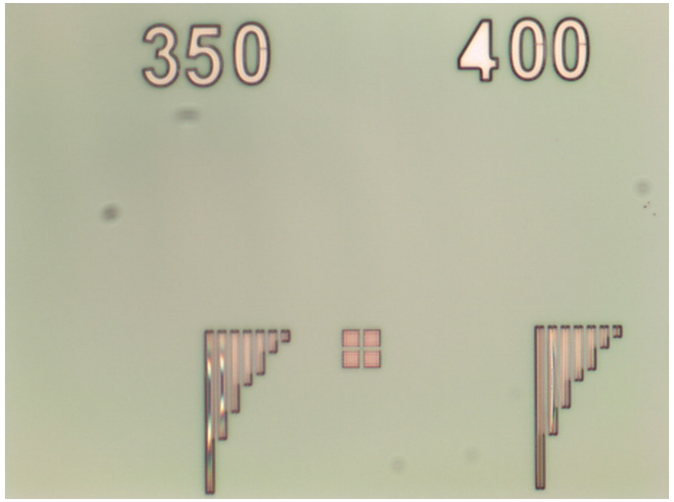
🟩 ARP 6200.9 (CSAR 62) -> 2000RPM 60sec -> ~270nm

🟦 Copolymer 13% -> 4500RPM 60sec -> ~700nm

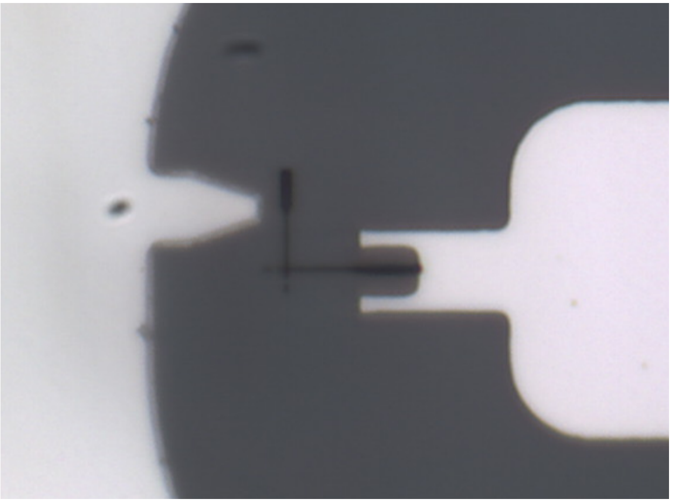
🟨 Al ~ 40nm

By using this dummy pattern one can achieve something similar to ‘differential dose’ or ‘local enhancement of undercut’

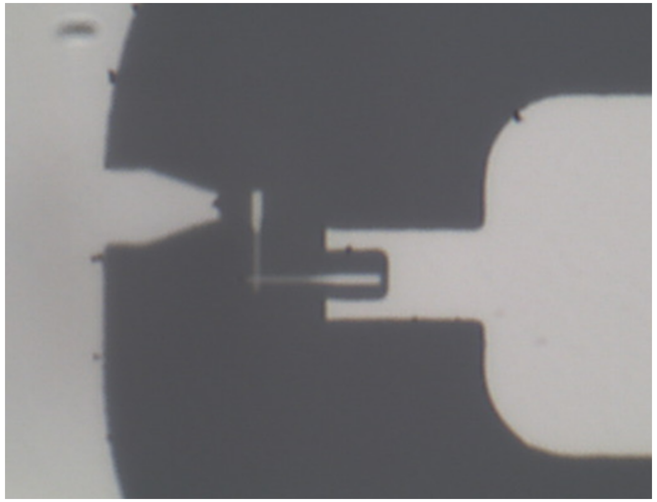
2nd EBL: JJ define



Undercut test structure



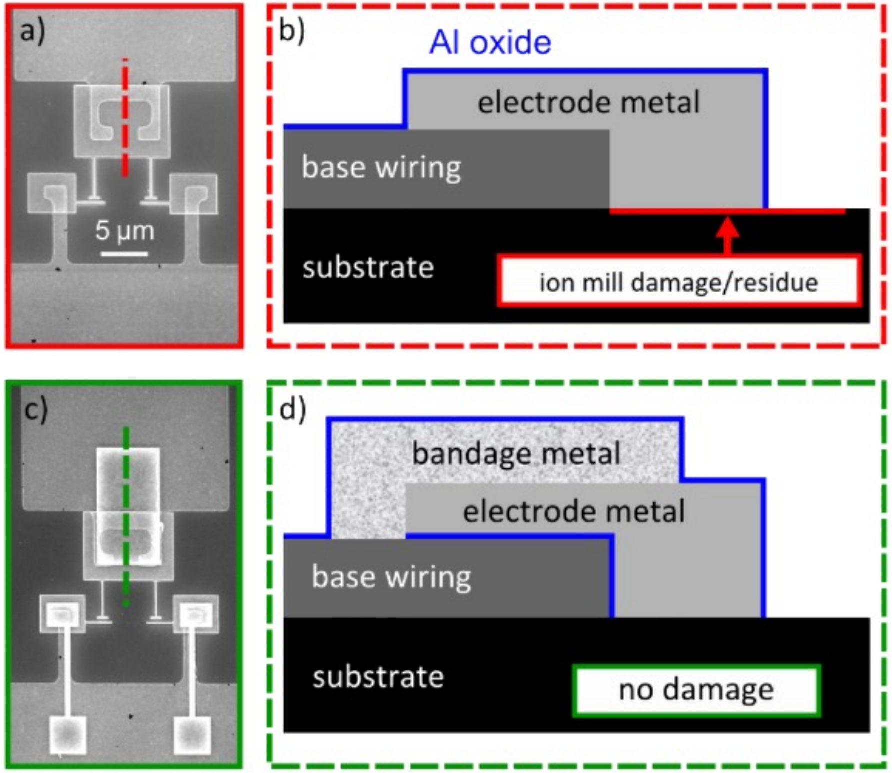
development



Lift-off

3rd EBL: patch define

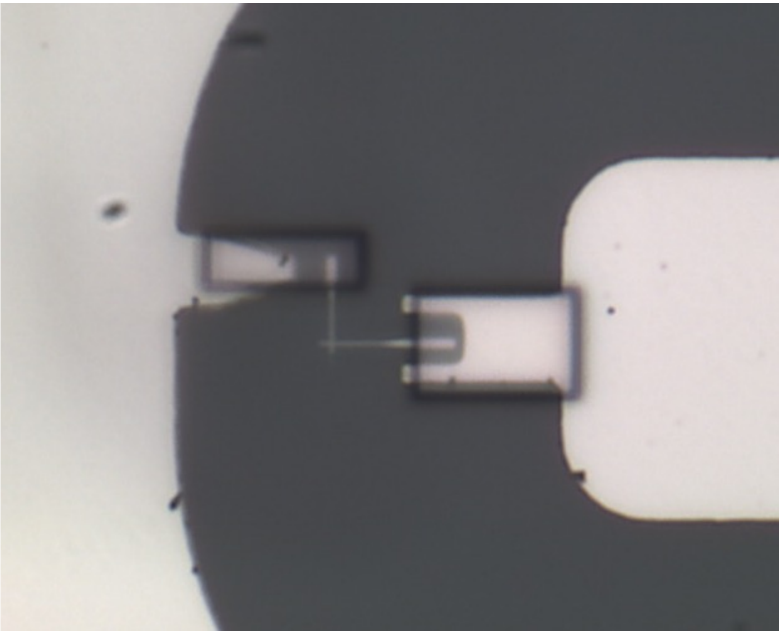
- Why do you need patch (or bandage)?
- Al quickly oxidized, forming good insulator
- Electrical contact between JJ and ground plane
- In-situ argon milling preferable
- But direct milling to the Si surface leads to unwanted TLS or other spurious effects



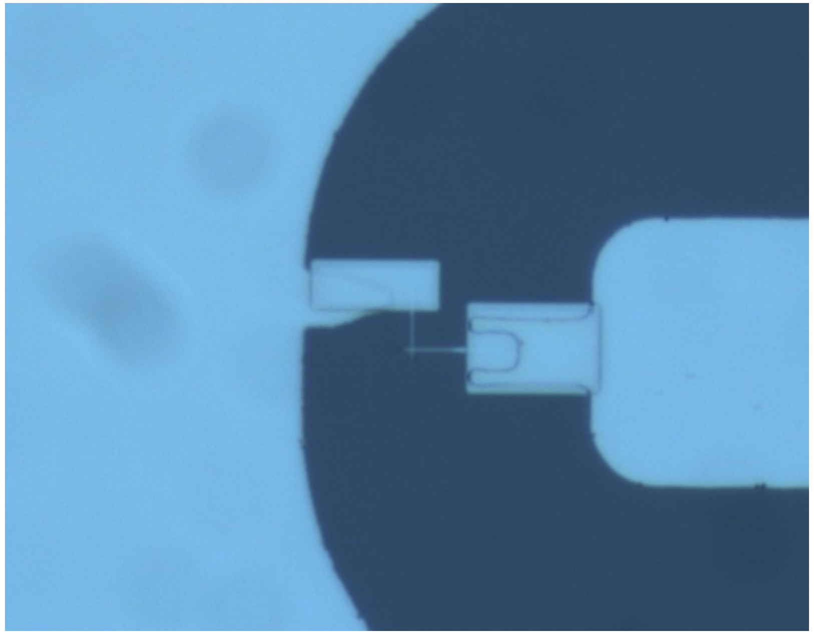
Appl. Phys. Lett. 111, 022601 (2017)

3rd EBL: patch define

- EBL, develop, descum -> evaporator
- Ar ion milling in-situ, Al path deposition
- Lift off, test JJ measurement, final



development



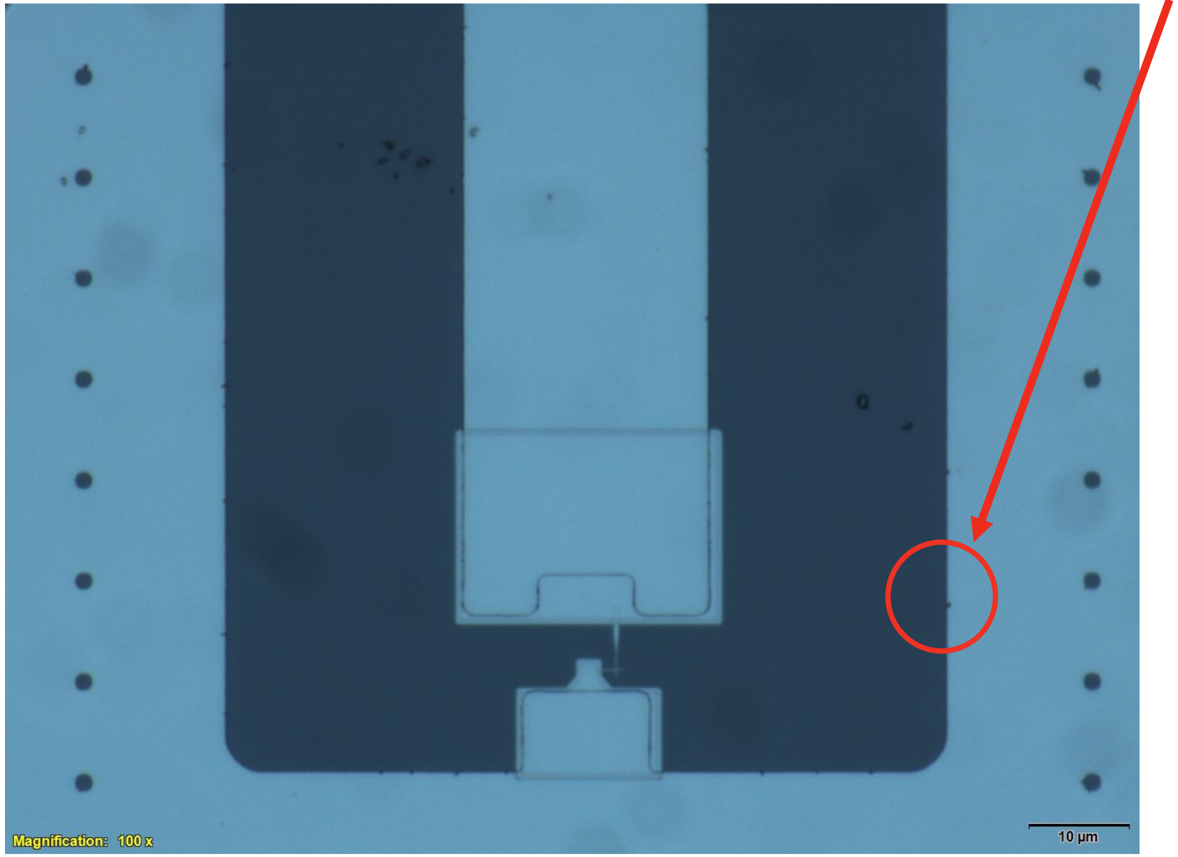
Lift-off

1) Al degradation over time

- Mainly observed along the line of etched pattern

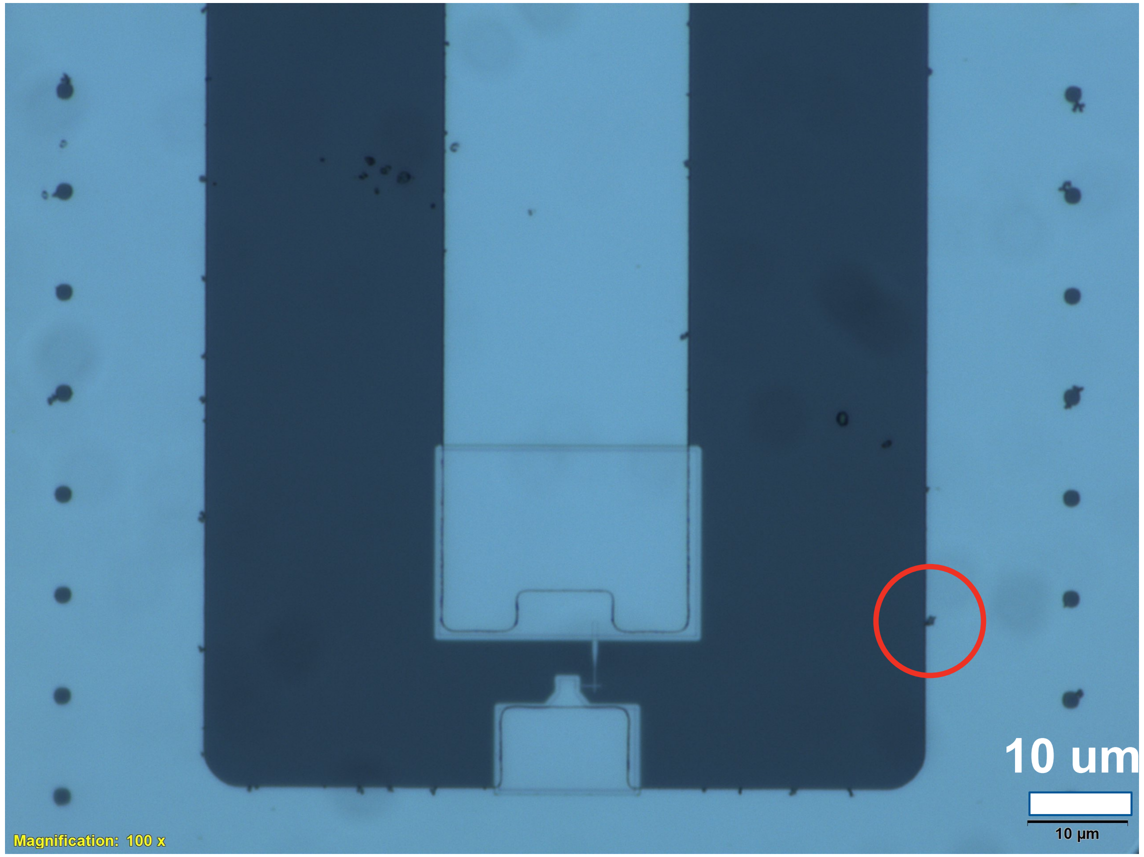
‘XMON20210503’ sample chip A, so-called 8kohm sample

Photo taken on 2021 May 21



Small black dot is there and it grows over time, 10 months

Photo taken on 2022 APR 01



Al degradation over time

- Mainly observed along the line of etched pattern

‘HUBBIT_2021_NOV_JJ_array’ after 4 months

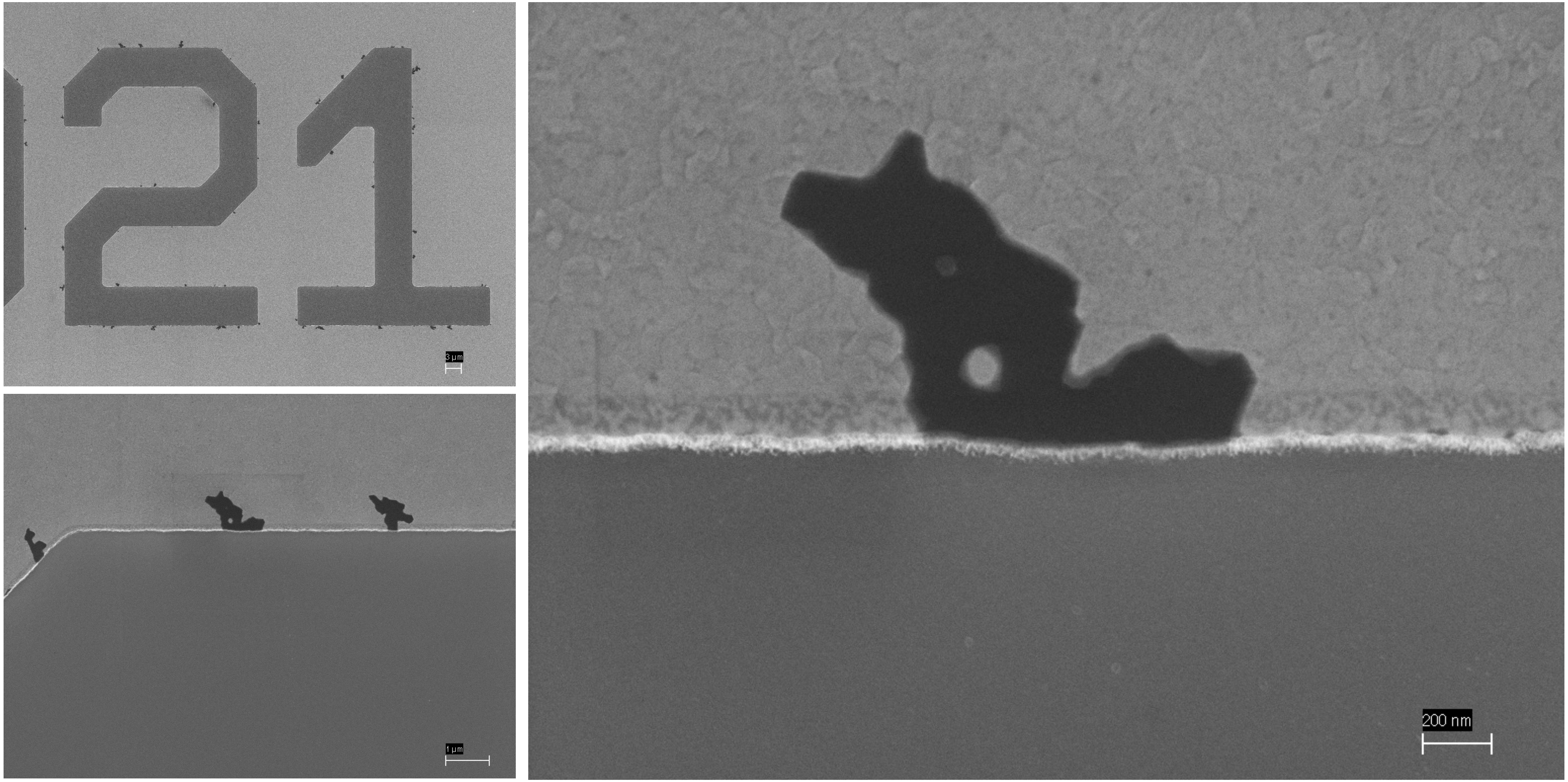
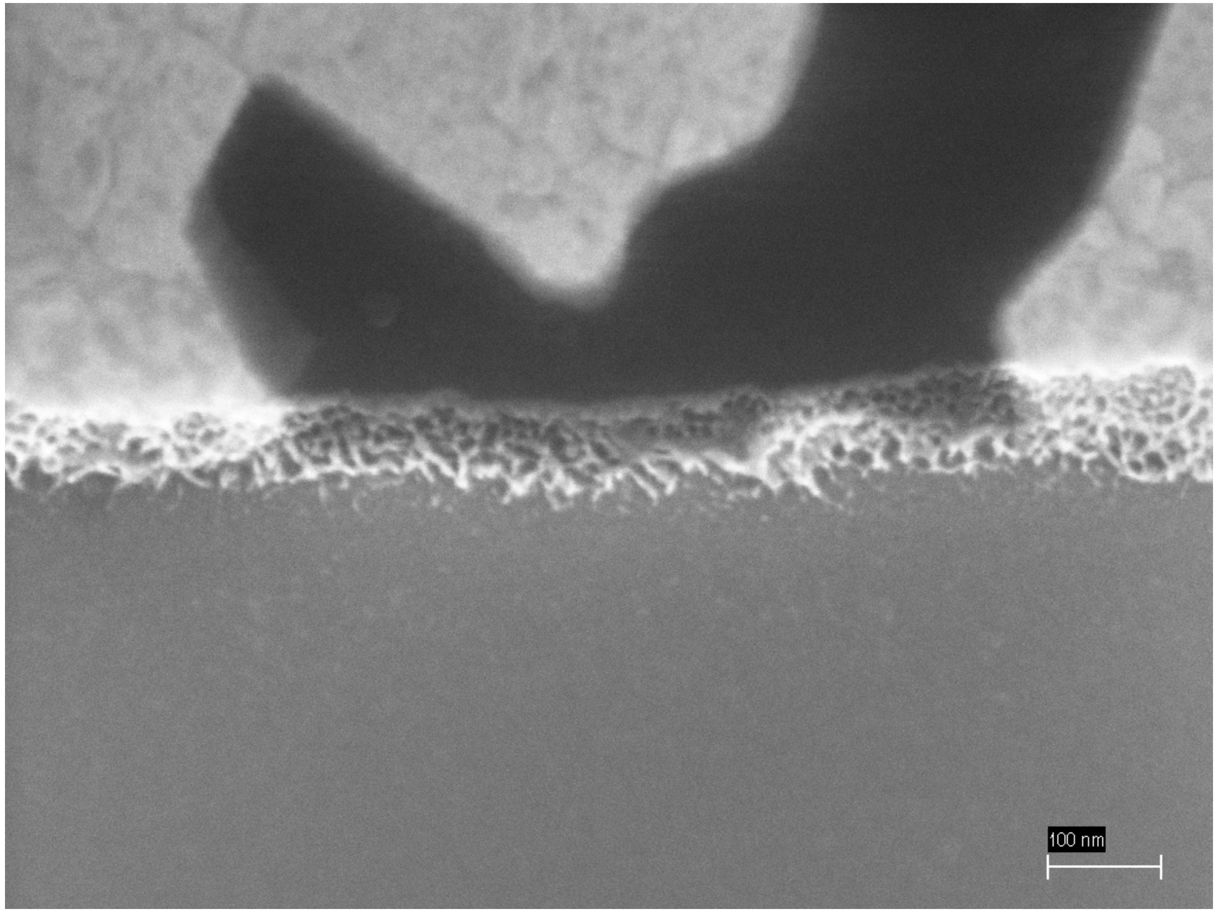


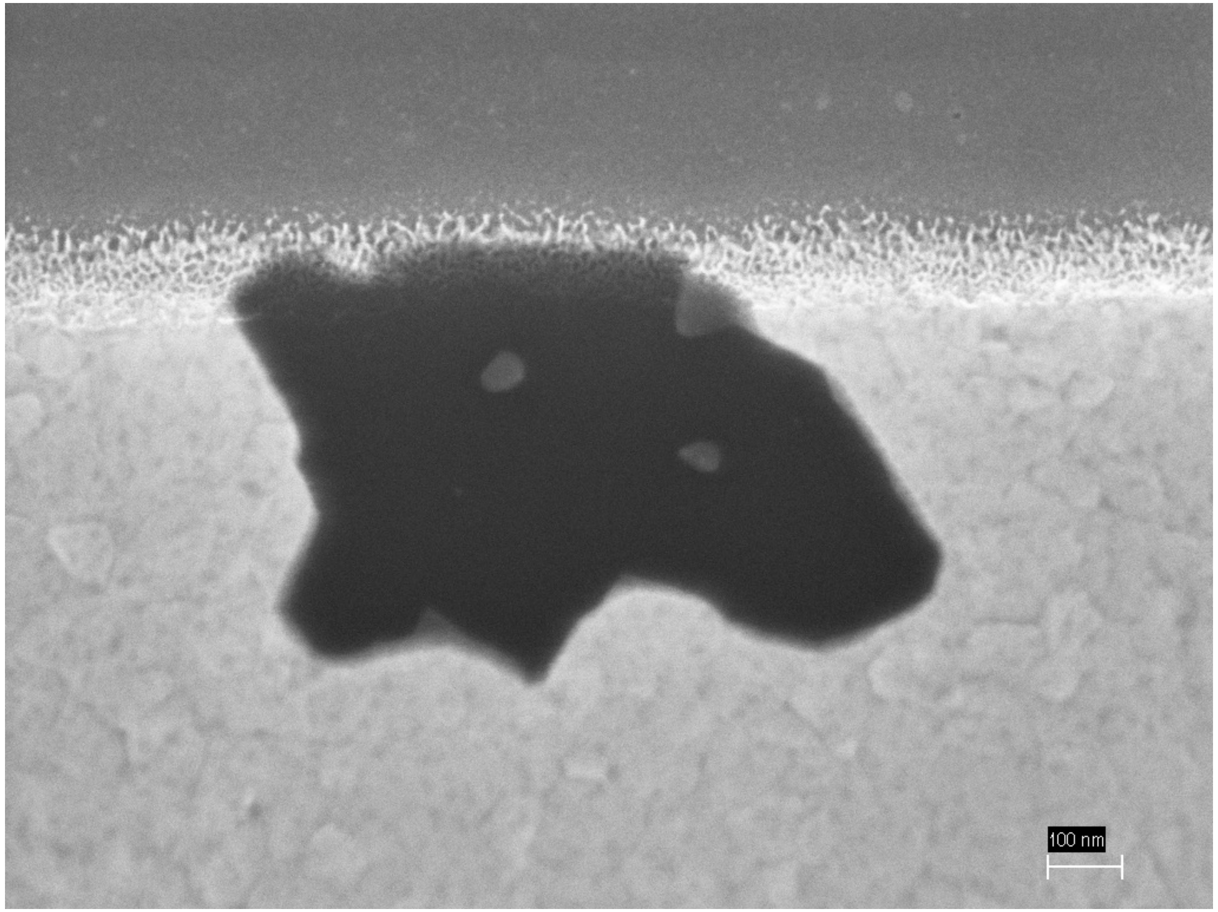
Photo taken on 2022 MAR 25

Al degradation over time

- Mainly observed along the line of etched pattern



‘HUBBIT_2021_NOV_JJ_array’ after 4 months

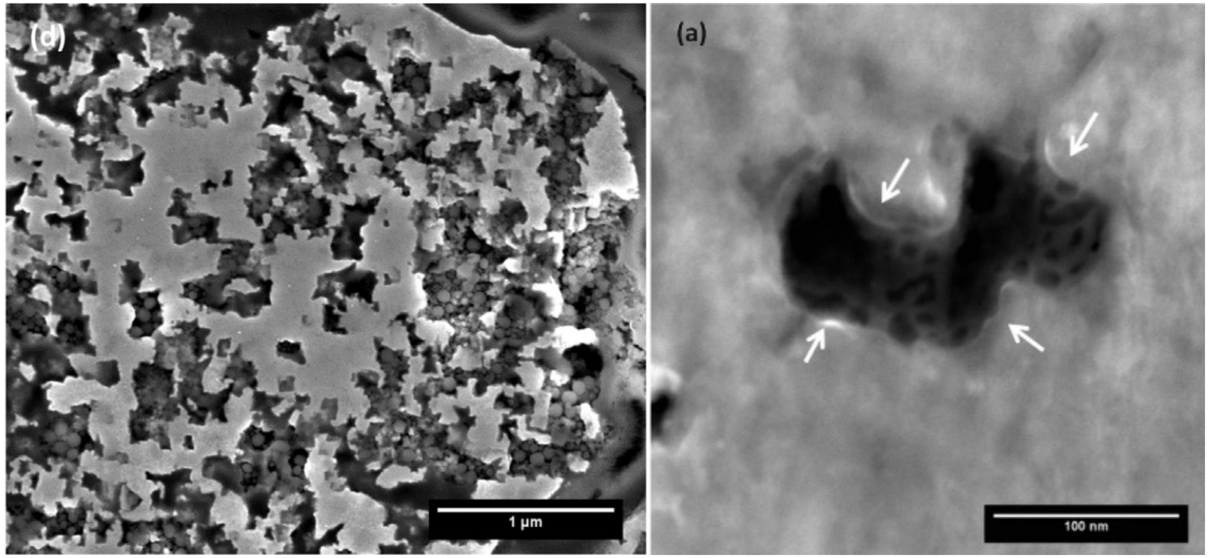


It is not void area, it is dielectric. Dark and semi transparent to electron beam.

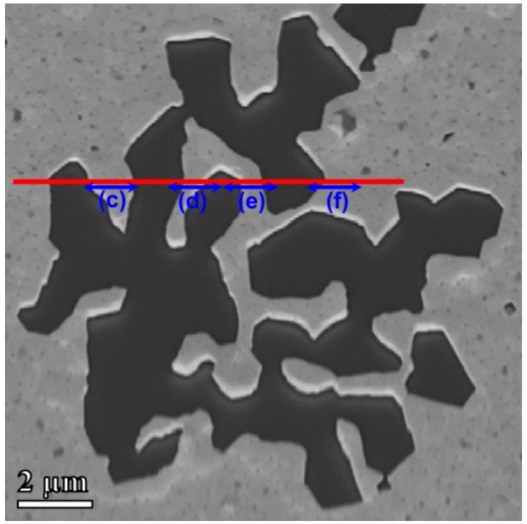
Granular shape, grain boundary -> implying this is chemical event

Photo taken on 2022 MAR 25

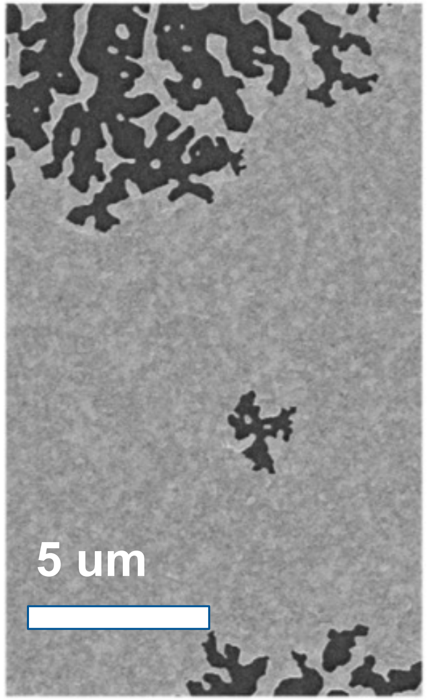
Similar to?



[1] Al alloy corrosion by NaCl solution



[2] anealed Au, film dewetting



[3] anealed AuPt

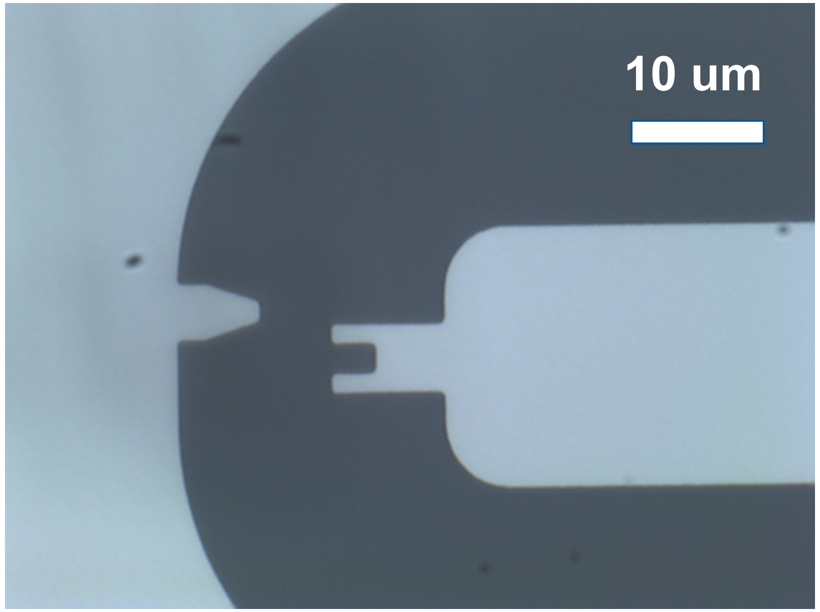
- Granular shape, grain boundary

[1] Materials Characterization **130**, 230-236 (2017)
[2] Acta Materialia **58** 6035–6045 (2010)
[3] Journal of Applied Physics **113**, 094301 (2013)

Al degradation over time

- not as pronounced at moment of right after etching (at least in OM)

‘HUBBIT_2022_JAN F2’



2m50s etched -> rinse -> 1m etch

Photo taken on 2022 MAR 30

right after etching

‘test HUBBIT_2022_JAN’

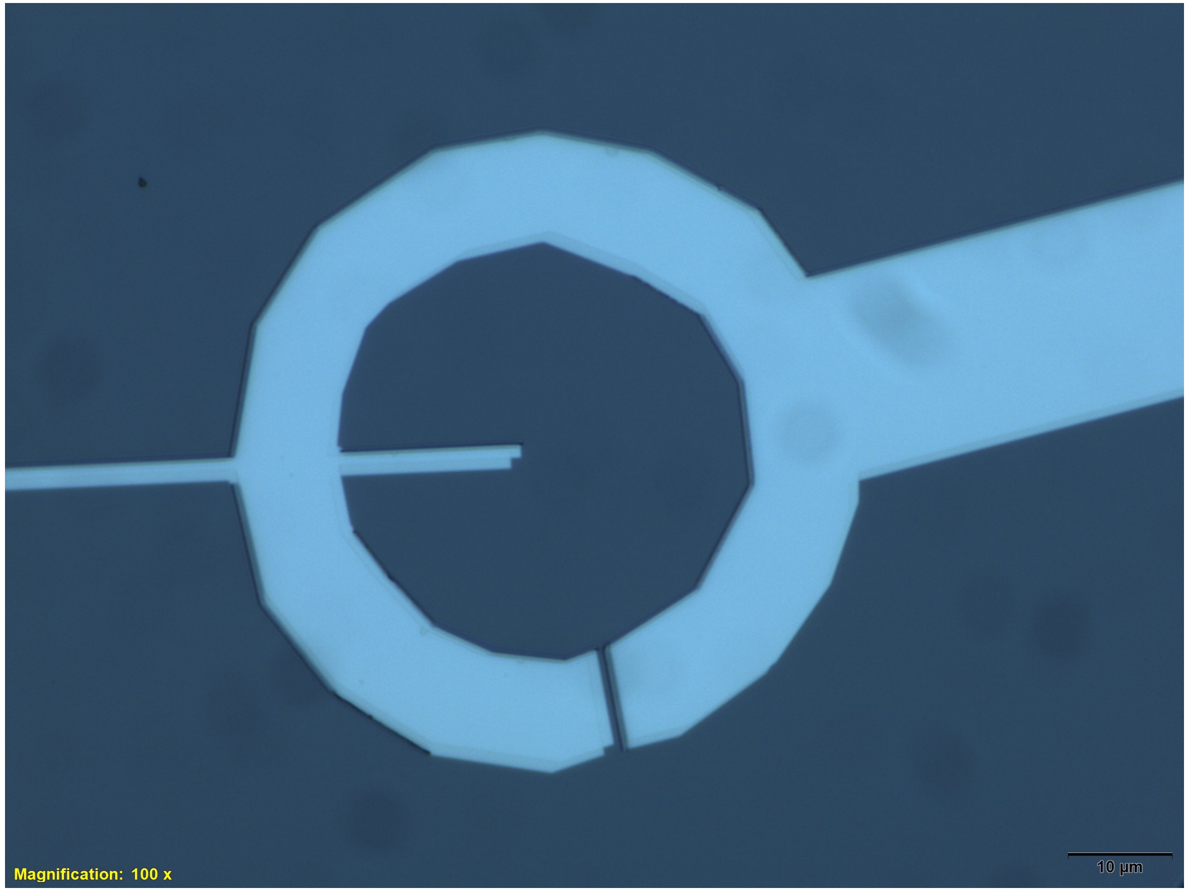
SEM image taken 6days after etch

3m etched -> rinse -> 1m etch

Al degradation over time

- No sign of it on the lift off sample

‘2021SET_v4_chip2’ after 11 months



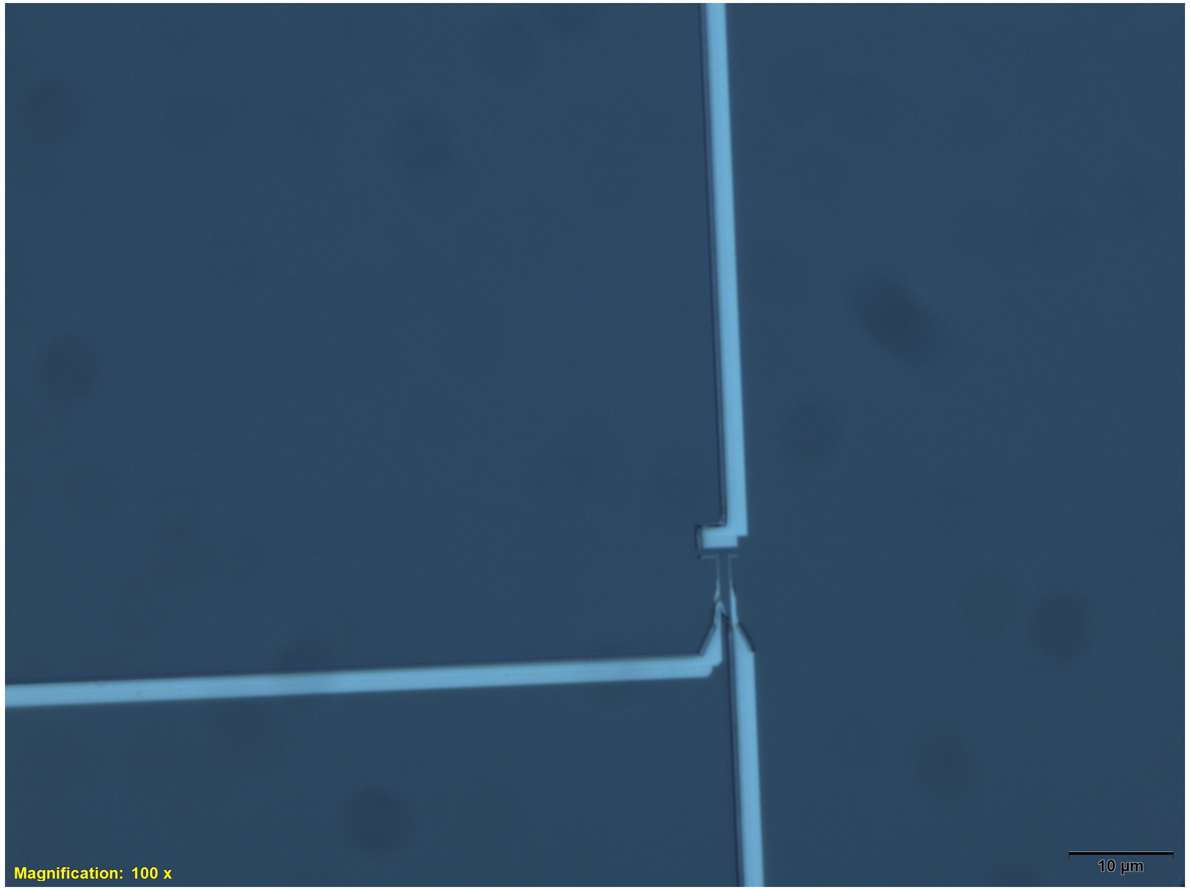
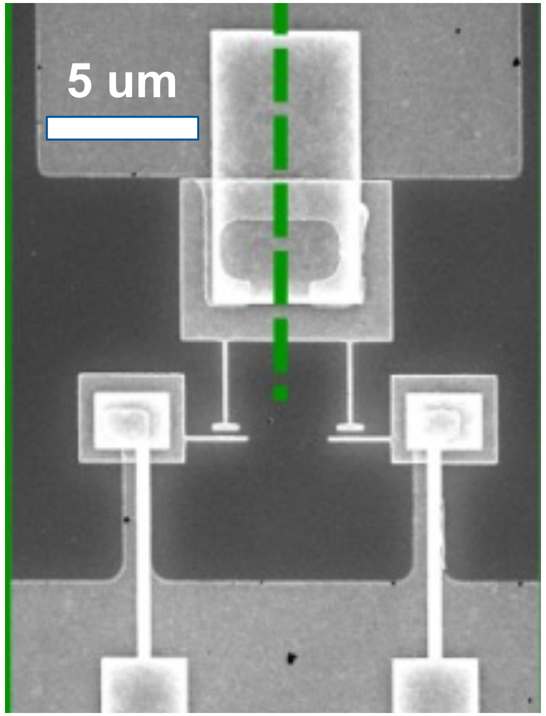
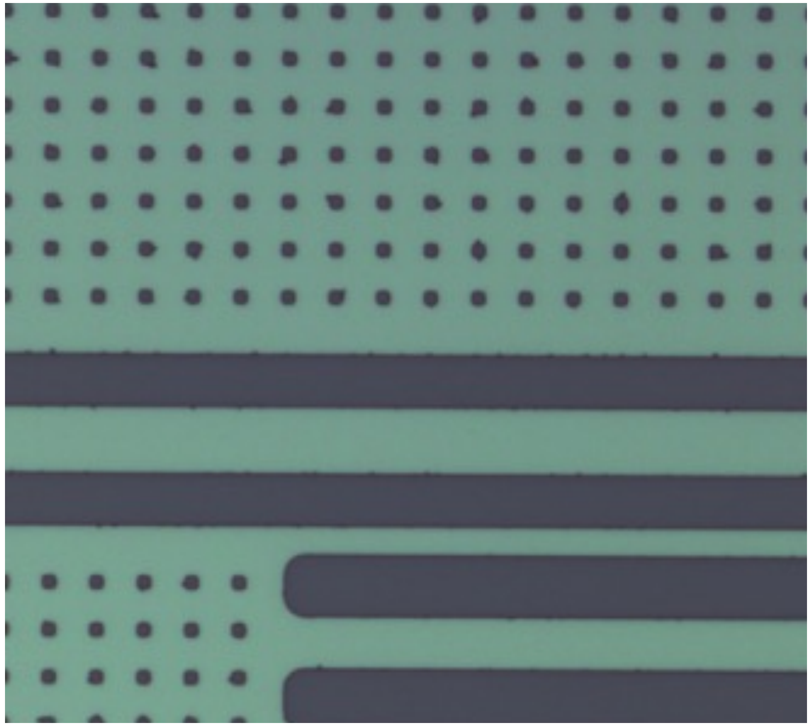


Photo taken on 2022 APR 01

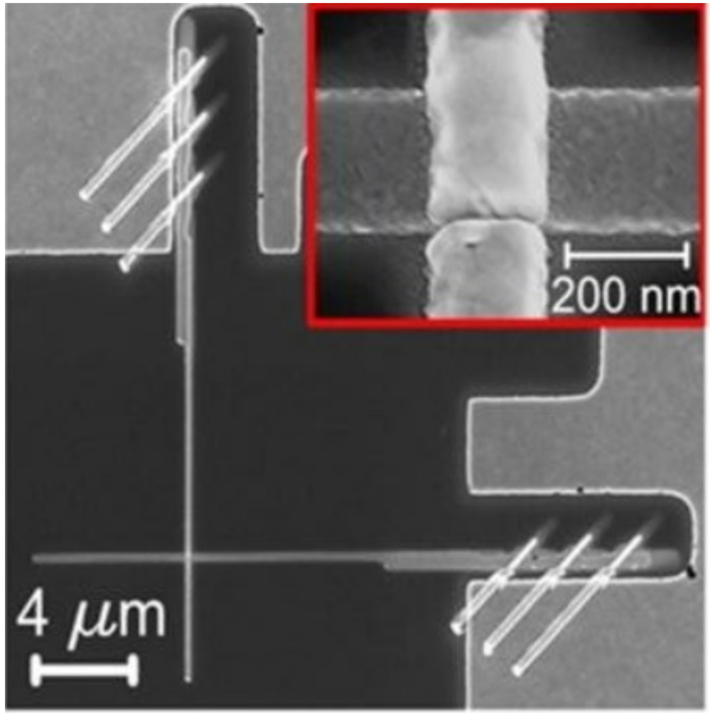
Al degradation over time, other group?



[1] UCSB Al etched with TMAH



[2] Charmers Al etched with acids



[3] Charmers Al etched with acids

black miniscule spots, not as severe as ours, also unknown how aged they are

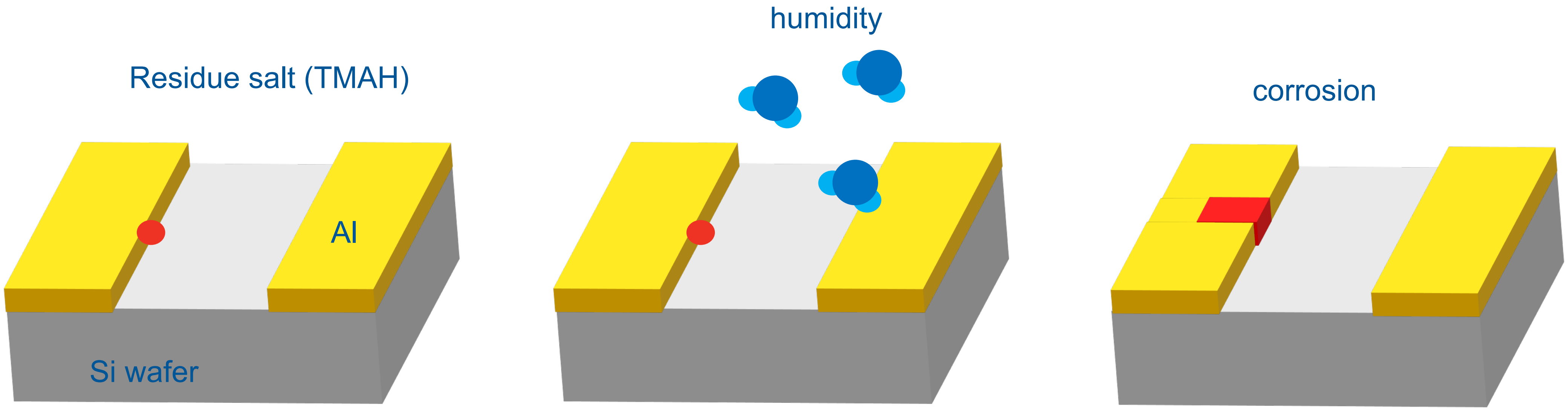
[1] A. Dunsworthet *al* Appl. Phys. Lett. 111, 022601 (2017)
[2] these of Andreas Bengtsson
[3] Appl. Phys. Lett. **118**, 064002 (2021)

Al degradation over time

- What is the source?

Possibly left over TMAH salt reacting with ambient humidity.

- Chip with more lithography steps (XMON from 2021 May) shows milder symptom, compared to only etched (HUBBITY 2021 NOV). Hint of unintentional cleaning by more lithography steps.
- Chip with no Al etch step is perfectly free from this degradation



Al degradation over time

Possible remedy

1) More intensive water rinse needed -> current 1m rinse in DI seems not enough.

* Current batch of HUBBIT JAN are additionally sonic agitated DI clean (2m) after mask removal

2) Sample should be polymer-coated while storage or vacuum stored, avoiding contact to humidity

3) Trying different chemical, Charmers most recent recipe, from 2020 phd These of Andreas Bengtsson,(and also UCSB) now they are using mixture of phosphoric, nitric, acetic acids. One for oxidizing, one for AlOx etch, one for wetting (so-called Aluminium etchant type A)

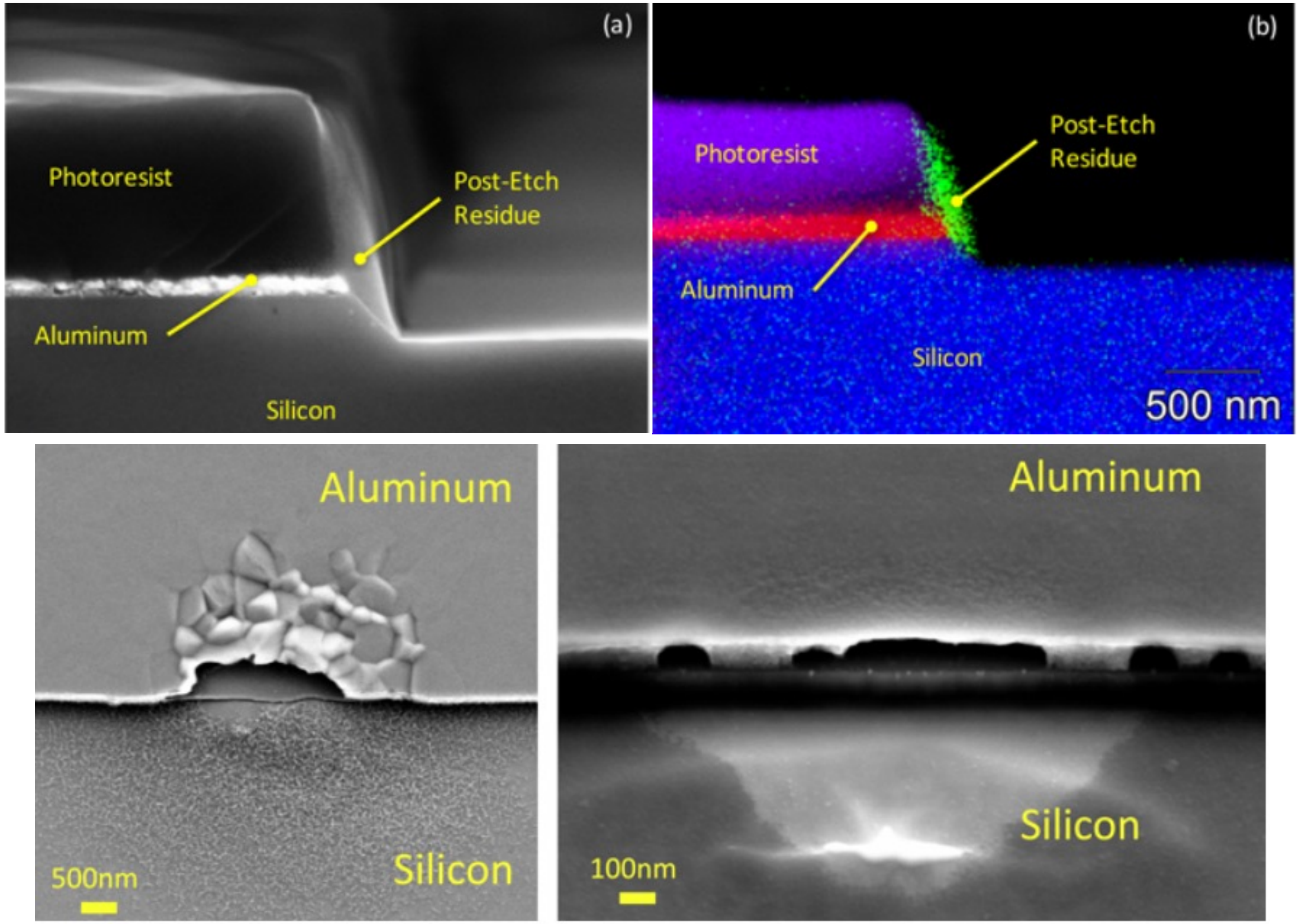
4) Finish whole process as soon as possible after Al etch step

5) Consume qubit sample immediately after fabrication.

More important question -> What is the impact on qubit performance?

Al degradation in ambient, Dry etch case

Cl based RIE etching -> Cl containing microscopic residue -> hydrochloric acid



C J K Richardson *et al* 2016 *Supercond. Sci. Technol.* **29** 064003

Now this issue seems relatively well known to community. (appears PhD thesis Charmers and UCSB)

Remedy,

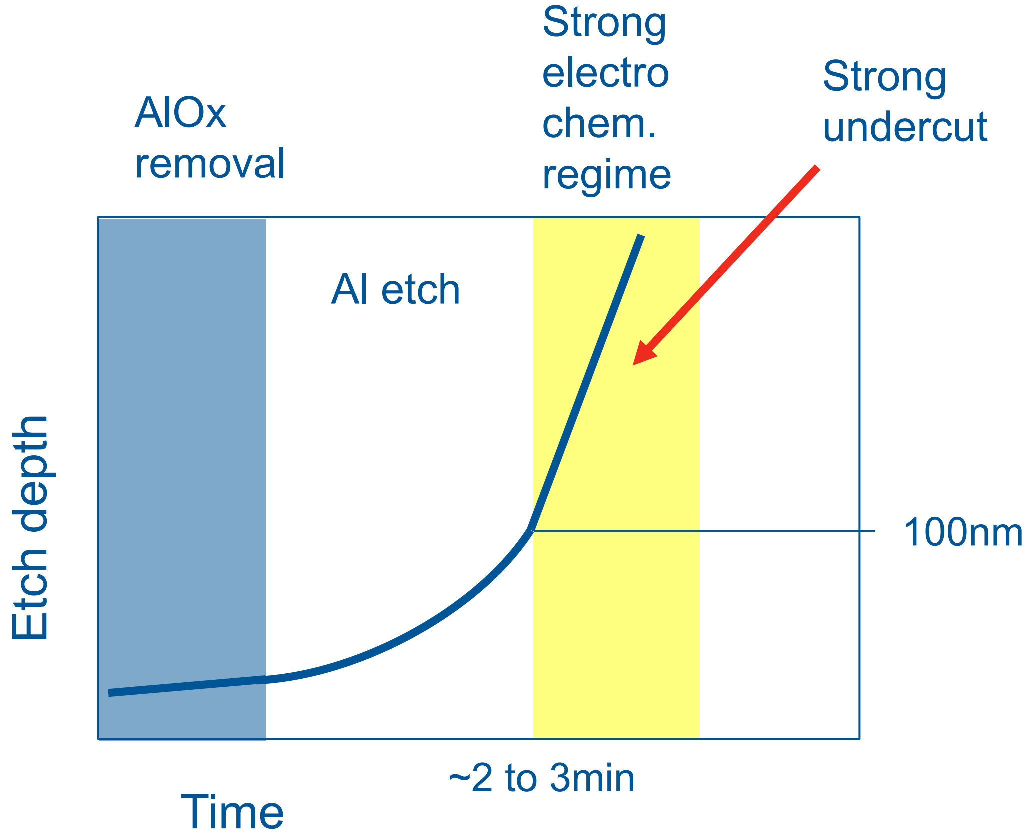
1) Intensive water rinsing.
2) Chemical treatment, base solution after RIE
3) Additional fluorine plasma to replace $\mathrm{Al}_y\mathrm{Cl}$ to $\mathrm{Al}_y\mathrm{F}$

Some comment on etch rate of Aluminium on Silicon wafer in TMAH

“The etch rate of the aluminum is electro-chemically enhanced by the silicon-aluminum interface and can be as much as 10 times faster than the etch rate of aluminum on a sapphire (Al2O3) substrate.” from UCSB, John Martinis group

A. Dunsworth*et al* Appl. Phys. Lett. 111, 022601 (2017)

- This explains why our etching process reproducibility is not amazing
- It makes sense to use nonconducting tweezer and glassware, to minimize any electrochemical process rooted from tweezer material
- it further explains why community moves to acid based special solution



*Graph not in real scale

Your Safety is more important than quantum

- Buddy system
- Don’t leave unlabelled & unattended chemical in the fab
- Personal Protective Equipment
- Know emergency exit

Hydrofluoric acid

- HF, Buffered Oxide Etcher: used for variety of oxide etch
- Colourless, order less, like water: use it in the dedicated space
- Etch SiO2: use Teflon ware
- When exposed: Hexafluorine, Calcium Gluconate gel (where you can see)
- Wear glove to avoid 2nd hand burn
- F containing gas used: ie. XeF2, possible HF build up at exhaust
- Danger: skin contact, inhalation
- Use protection and check whether you can use lower concentration (and usually you do!)
- Anything with "fluorine, fluoride" … check MSDS
- Waste stored separately

Piranha solution

- Sulfuric acid + hydrogen peroxide
- Strong oxidizer: Clean wafer from organic contamination
- Always adding hydrogen peroxide to sulfuric acid, never in reverse order
- Extremely exothermic: mixing gentle and slowly
- hydroxylate surfaces (by adding –OH groups), making highly hydrophilic (water-compatible)
- Large amount of contaminant will cause violent bubbling gas and explosion
- You can purchase ready made product (Nano strip)
- Use protection and check whether you really needs this

Blackout safety

Luminous evacuation route sign

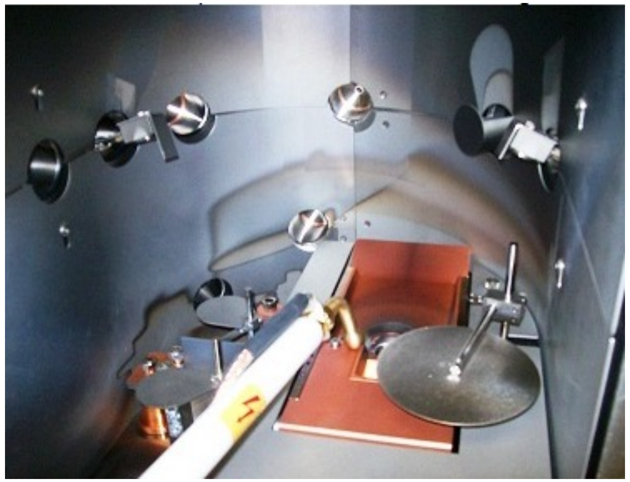
Auto start lamp

- If you are a PI or lab manager : equip with blackout safety
- Cleanroom in the dark is perfect place to have accidents

Health and safety

- Fume hood: flow sensor
- Gas leak sensor: Metal etching RIE might have Chlorine gas
- Oxygen level sensor: when suffocation possible, ie. LN2
- Think about the density of target gas: location of sensor

- Electric shock: evaporator



- Do not mix Acid and organic waste
- Always add acid to water, never reverse (exception piranha)
- Have pH strips in the fab

Thank you for your attention